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RENNER SARTÓRIO CAMARGO

DOCTORAL THESIS

A NOVEL CASCADED MULTILEVEL CONVERTER TOPOLOGY BASED ON THREE-PHASE CELLS

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Ph.D. Thesis presented to the Electrical Engineering Postgraduate Program of the Federal University of Espírito Santo, as a partial requirement to obtain the degree of Doctor in Electrical Engineering, in the area of concentration: Energy Processing and Electrical Systems.

Advisor: Prof. Dr. Lucas Frizera Encarnação
Co-advisor: Prof. Dr. Emilio José Bueno Peña
Co-advisor: Prof. Dr. Domingos Sávio Lyrio Simonetti

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COMISSÃO EXAMINADORA

Prof. Dr. Lucas Frizera Encarnação - Advisor
PPGEE - Féderal University of Espírito Santo

Prof. Dr. Emilio José Bueno Peña - Co-Advisor
University of Alcalá

Prof. Dr. Domingos Sávio Lyrio Simonetti - Co-Advisor
PPGEE - Federal University of Espírito Santo

Prof. Dr. Luis Guilherme Barbosa Rolim
Federal University of Rio de Janeiro

Prof. Dr. Mauricio Aredes
Federal University of Rio de Janeiro

Prof. Dr. Weder Tótola Nunes
Federal Institute of Espírito Santo

Prof. Dr. Walbermark Marques dos Santos
Federal University of Espírito Santo

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“Nobody ignores everything.
Nobody knows everything.
That’s why we always learn.”
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into the arms of the Father in Heaven
due to the Coronavirus pandemic (Covid-19)
that is plaguing the world.

Abstract

Due to the structural characteristics of modern electrical grids, the use of equipment based on power electronics to guarantee its perfect functioning has grown sharply, encouraging the study and development of equipment based on these technologies like converters with multiple voltage levels, known in the literature as multilevel converters.

Multilevel converters based on H bridge cells, known in the literature as CHB (Cascaded H bridge Converter) are the most outstanding among this converters category, however, the natural switching of the multilevel CHB converter in specific configurations, such as a back-to-back connection (CHB-B2B), presents several short-circuit states, making its performance unfeasible or limiting. This issue may require additional stages of isolation, increasing its implementation cost and reducing its competitiveness.

Under these circumstances, this work proposes a new multilevel converter topology based on H bridge cells, without isolation stages, with three-phase characteristics and superiority in some metrics compared to a CHB of the same specifications. It also has a lower number of components, lower construction cost, and similar performance.

This newly proposed topology, named SDC-CHB (Cascaded H Bridge Converter with Single DC-link), also features several short-circuit states as well as CHB. However, the use of graph theory and model-based predictive control (MPC) enables the inhibition of the short-circuit stages inherent to the SDC-CHB topology.

This work is also dedicated to the mathematic study and the mapping of the SDC-CHB short circuit states in a STATCOM as a power electronic application, and comparing its performance with this device using a CHB converter with similar characteristics.

This topology was subjected to simulations in Simulink Matlab® software for data analysis and later implemented on a hardware-in-the-loop (HIL) real-time platform from the manufacturer OPAL-RT, model 5700, to prove its applicability and to validate the proposal.

To analyze the efficiency of the converter, measurements of losses by conductivity and switching were carried out using the PLECS® Plexim software, where the energy consumption of the converter in different modes of operation can be observed.

Keywords: Multilevel Converters; Cascaded H Bridge Converter (CHB); Cascaded H Bridge Converter with Single DC-link (SDC-CHB); Model-based Predictive Control (MPC); Simulink Matlab; Hardware-in-the-Loop (HIL); OPAL-RT.

Resumo

Devido às características estruturais das redes elétricas modernas, a utilização de equipamentos baseados em eletrônica de potência para garantir seu perfeito funcionamento tem crescido fortemente, incentivando o estudo e desenvolvimento de equipamentos baseados nessas tecnologias como conversores multinível.

Os conversores multiníveis baseados em células em *H bridge*, conhecidos na literatura como *CHB* (*Cascaded H bridge Converter*) são os que mais se destacam nesta categoria de conversores, porém, a comutação natural do *CHB* multinível em configurações específicas, como em back-to-back (*CHB-B2B*), apresenta vários estados de curto-circuito, tornando seu desempenho inviável ou limitante. Este tipo de operação pode requerer estágios adicionais de isolamento, aumentando seu custo de implantação e reduzindo sua competitividade.

Assim, este trabalho propõe uma nova topologia de conversor multinível baseada em células em *H bridge*, sem estágios de isolamento, com características trifásicas e superioridade em algumas métricas em relação a um *CHB* de mesmas especificações. Também apresenta menor número de componentes, menor custo de construção e desempenho semelhante.

Esta nova topologia, denominada *SDC-CHB* (*Cascaded H Bridge Converter with Single DC-link*), também apresenta vários estados de curto-circuito, bem como o *CHB*. No entanto, o uso da teoria dos grafos e do controle preditivo baseado em modelo (*MPC – Model Predictive Control*) possibilita a inibição dos estágios de curto-circuito inerentes ao *SDC-CHB*.

Este trabalho também se dedica ao estudo matemático e ao mapeamento dos estados de curto-circuito do *SDC-CHB* em uma aplicação de eletrônica de potência como o *STATCOM*, e à comparação do desempenho deste dispositivo utilizando um conversor *CHB* com características semelhantes.

Para validar a proposta, esta topologia foi submetida a simulações no software Simulink Matlab® para análise de dados e implementada em plataforma de tempo real *hardware-in-the-loop* (*HIL*) do fabricante OPAL-RT, modelo 5700, para comprovar sua aplicabilidade.

Para análise do rendimento do conversor, foram efetuadas medições das perdas por condutividade e chaveamento através do software PLECS® da empresa Plexim, onde pode-se observar o gasto energético do conversor nos diferentes modos de operação.

Palavras-chave: Conversores Multinível; Conversor em Cascata com ponte-H (CHB); Conversor em Cascata com ponte H e elo CC compartilhado (SDC-CHB); Controle Preditivo baseado em Modelo (MPC); Simulink Matlab; Hardware em Tempo Real (HIL); OPAL-RT.

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Abbreviations

Symbol

Symbol	Description
a, b, c, n	$Phases\ a, b, c\ and\ neutral$
C	$Capacitor$ / *Capacitance*
C_{DC}	$DC - link\ Capacitor$
D	$Diode$
$\frac{di}{dt}$	$Derivative\ of\ current\ with\ time$
e, U	$Voltage$
g	$Cost\ Funciton$
I, i	$Current$
$k-1$	*Previous time instant*
k	$Actual\ time\ instant$
$k+1$	$Next\ time\ instant$
$k+2$	$Next\ two\ time\ instants$
L, l	$Inductance$
m	$Number\ of\ voltage\ levels$
MOD	$Module$
N	$Number\ of\ capacitors$
n_s	$Number\ of\ switching\ states$
P	$Active\ Power$
p	$Power\ losses$
Q	$Reactive\ Power$
S	$Semicondutor\ switch$ / Switching vector
T_s	$Time\ step$
TWh	$TeraWatt - hour$
U_{DC}	$Capacitor\ /\ DC - link\ Voltage$
var	$Reactive\ Volt - Ampére$
W	$Weight\ in\ function\ cost$
x	$Variable$

ω	$Angular\ grid\ frequency$
ΔU	$Voltage\ range$

Overlapping symbols

Symbol	Description	Example
—	$Switch\ state\ negation$	$\overline{S_x}$

Superscript and subscript symbols

Symbol	Description	Example
$1,2,\ldots,x$	$Number\ Index$	C_1
$3\emptyset$	$Three-phase$	$C_{3\emptyset}$
a,b,c,n	$Phase\ index$	S_{ax}
c	$Carrier$	f_c
CHB	$Cascaded\ H\ Bridge\ Converter$	C_{CHB}
$damp$	$Damping$	l_{damp}
DC, dc	$Direct\ Current$	$U_{DC}\ /\ U_{dc}$
en	$Penalty$	P_{en}
i	$Individual\ value$	C_{iCHB}
$k-1$	$Previous\ time\ instant$	x^{k-1}
k	$Actual\ time\ instant$	x^k
$k+1$	$Next\ time\ instant$	x^{k+1}
$k+2$	$Next\ two\ time\ instants$	x^{k+2}
$loss$	$Losses$	p_{loss}
min	$Minimum\ value$	g^{min}
N	$Negative\ current\ /\ Prediction\ Index$	$i_N\ /\ g^N$
Nom	$Nominal$	S_{nom}
opt	$Optimum\ Value$	S^{opt}
p	$Predicted\ variable$	x^p

s	$Number\ of\ switching\ states\ /\ source\ /\ step$	$n_s\ /\ e_s\ /\ T_s$
$samp$	$Sampling$	T_{samp}
$T\ /\ TOT$	$Total$	$P_T\ /\ C_{TOT}$
th	$Index\ of\ values$	$(k+2)^{th}$
$SDC-CHB$	$Cascaded\ H\ Bridge\ Converter\ with\ Single\ DC-link$	$C_{SDC-CHB}$
$*$	$Reference$	P^*

Acronyms and Abbreviations

Acronym / Abbreviation	**Description**
$AFTC$	$Active\ fault-tolerant\ controller$
AC	$Alternate\ Current$
$AHMC$	$Asymmetric\ hybrid\ multilevel\ cells\ converter$
$B2B$	$Back-to-Back$
$CCMC$	$Capacitor-Clamped\ Multilevel\ Converter$
CCS	$Continuous\ Control\ Set$
CHB	$Cascaded\ H\ Bridge\ Converter$
DC	$Direct\ Current$
$DC-DC$	$Direct\ Current\ to\ Direct\ Current\ Converter$
$DCMC$	$Diode-Clamped\ Multilevel\ Converter$
$DFIG$	$Doubly-fed\ Induction\ Generator$
$eFPGASIM$	$OPAL-RT\ Simulation\ Platform\ based\ on\ FPGA$
$EMPX$	$Explicit\ MPC$
$FACT$	$Flexible\ AC\ Transmition\ System$
FCS	$Finite\ Control\ Set$
$FPGA$	$Field\ Programmable\ Gate\ Array$
GPC	$Generalized\ Predictive\ Control$
HIL	$Hardware-in-the-loop$
I/O	$Input\ /\ Output$
$Matlab®$	$Mathematical\ Software$

$MHMC$	$Mixed-level\ Hybrid\ Multilevel\ Cells\ Converter$
MMC	$Modular\ Multilevel\ Converter$
MPC	$Model\ Predictive\ Control$
OFF	$Turn\ OFF\ switch$
ON	$Turn\ ON\ switch$
$OPAL-RT$	$Hardware-in-the-loop\ platform$
OSS	$Optimal\ Switching\ Sequency$
OSV	$Optimal\ Switching\ Vector$
$PFTC$	$Passive\ fault-tolerant\ controller$
$PSPWM$	$Phase\ shifted\ PWM$
PWM	$Pulse\ Width\ Modulation$
RMS	$Root\ Mean\ Square$
$SDC-CHB$	$Cascaded\ H\ Bridge\ Converter\ with\ Single\ DC-link$
$Simulink$	$Simulation\ Software$
SST	$Solid\ State\ Transformer$
$STATCOM$	$Static\ Synchronous\ Compensator$
THD	$Total\ Harmonic\ Distortion$
$UPQC$	$Unified\ Power\ Quality\ Conditioner$

Chapter 1: Introduction

In the last decades, the demand for electric energy has grown globally at high rates. One of the causes is the accentuated use in the industrial parks of high-power equipment, such as driving motors, laminators, pumps, fans, and compressors. For example, the consumption of electricity in Brazil in the last fifteen years increased by approximately 45%, reaching more than 481 TWh in 2019 [1]. Besides, the incentive to decentralized generation and the need for better integration of power generation systems, including renewable energy sources, present significant challenges for electric system operators [2, 3].

The use of advanced power electronics devices is essential to meet requirements for the operation of the modern grids, including power quality issues [4], for example, the proper integration of the energy matrix [5], the electrical systems stability maintenance, or even the compensation of reactive power in offshore wind farms. Also, the smart grid concept is increasingly present in the electrical infrastructure, and such equipment can add resilience to power systems, making their responses to emergencies more robust [6, 7].

This high-power level requires an increase in the voltage levels involved to reduce costs, especially concerning the gauge of electrical conductors to provide appropriate adaptation to the installation rules to mitigate losses due to joule effects. Such an increment in the voltage levels can reach the physical limit of the semiconductor switches, making it impossible, in some cases, to drive some equipment through a single device (or conventional converters) connected directly to medium voltage [3, 8, 9].

Due to this technological deficit, several studies were carried out to develop specific converters to meet the growing demand for high-power equipment. This barrier stimulated the interest of the power electronics community, identifying in the multilevel converters a great potential for overcoming this scientific barrier of semiconductors. [10, 11, 12, 13].

In this way, the multilevel converters presented in the literature, due to their various output voltage levels, present several advantages over conventional converters, such as the ability to synthesize higher output voltage levels; use of lower power semiconductor devices [2]; presentation of a greater number of levels in the output voltage resulting in a waveform with less harmonic content; decreased voltage stress on semiconductor switches; and reduction of switching frequency per component [11, 14].

Despite the operational benefits of multilevel converters, its main disadvantage is the high cost due to the number of components as the number of voltage levels increases, limiting their use in higher value-added applications [15]. Besides, some topologies also present great complexity in controlling the capacitor's DC-links voltages, making it quite tricky to implement in some cases [7].

1.1 Problem Definition

This thesis is motivated by the presentation of a new modular multilevel converter topology at a lower cost and capable of being used in a greater number of applications.

Possible applications of the new modular multilevel converter topology, replacing the classic CHB:

- Back-to-Back (B2B) converters for driving motors or static loads [16];
- Solid State Transformers (SST) for connecting a wide variety of energy sources to the power grid [17];
- Unified Power Quality Conditioners (UPQC) to actively improve the quality of electricity [18];
- Synchronous Static Compensators (STATCOM) for reactive power compensation, mitigating harmonics, improving power factor [19, 20]; and others.

In most cases, multilevel converters, depending on the voltage level involved, connect the rectifier stages to inverter stages through a DC-link. Need for galvanic isolation provided by transformers to avoid short-circuit stages characteristic of the topologies used. [21, 22].

New topology, with a three-phase structure, using fewer capacitors, no isolation stages, and lower implementation cost than CHB. However, the new topology also presents short-circuit stages when used in switching based on PWM modulation, which requires a control strategy to activate its switches [11].

Besides, a solution for eliminating short-circuit states based on the Model Predictive Control (MPC) without losing the converter controllability and power quality is presented., which is capable of eliminating the short circuit stages in the capacitors and exploring all the remaining switching states without losing the converter controllability and the power quality.

1.1.1 SDC-CHB Application

With the modern regulation regarding the generation and electric energy commercialization, and new restrictions imposed by economic and environmental factors, there was an increase in the participation of wind generation in the power system [23].

Most wind farms use doubly-fed induction generator (DFIG) systems for several facilities this machine offers, such as increased efficiency and the ability to decouple the control of active power and reactive power for better integration in the power grid. However, because the DFIG has the stator directly coupled to the grid, being more sensitive to faults and unstable wind characteristics, power plants based on wind generation have stability problems when connected to the power grid. STATCOM is presented as a good solution for dynamic reactive power compensation according to grid voltage variation under these conditions.

In addition to wind-farm applications, STATCOM can act as a voltage regulator, power flow control, transient stability and dampening power oscillation, and others. Besides, the use of H bridge cells is a good option for STATCOM applications due to the presence of the DC-link capacitors, which help to reduce the current THD, keeping its amplitude index close to 1.0, especially when these devices provide reactive power to the system [23]. An example of this application is shown in Figure 1-1.

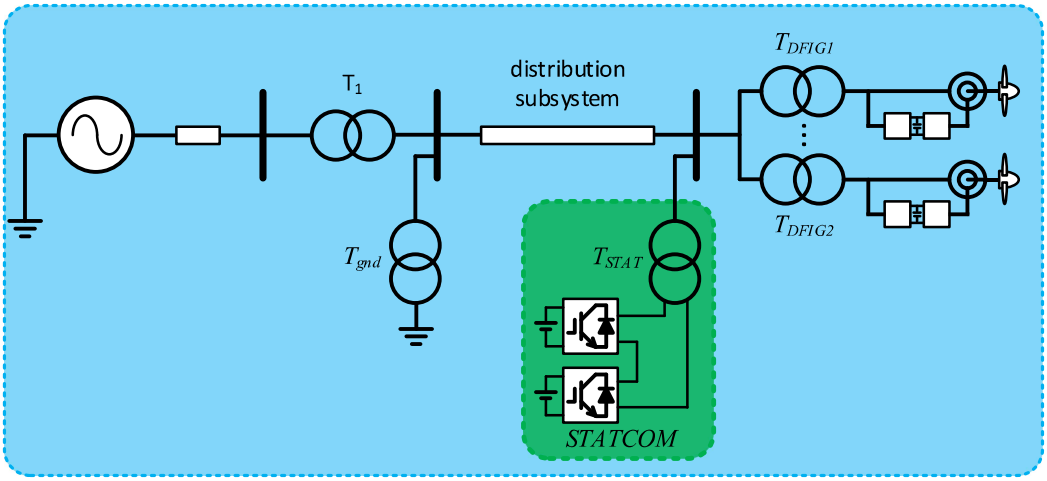


Figure 1-1– STATCOM application in a wind farm system.

Due to the modernity of applications that require actuators based on power electronics, and because of its importance for modern electrical systems, STATCOM was chosen to prove the proposed SDC-CHB topology's functioning and validate the switching strategy based on MPC to eliminate the short-circuit states inherent to this structure.

1.2 Methodology

The main objective of this thesis is to propose a modular multilevel converter with a reduced number of components, three-phase structure, and operating parameters compared to CHB of the same specifications, without isolation stages used in back-to-back configurations, proving its technical feasibility.

The main contributions presented by this work to achieve the main objective are listed: it is listed:

- The development of a mapping strategy and analysis of short-circuit stages inherent to the proposed SDC-CHB (Cascaded H Bridge Converter with Single DC-link) topology, based on graph theory;
- The mathematical development of a STATCOM based on SDC-CHB;
- The development of a control strategy based on MPC that provides perfect functioning of the SDC-CHB no occurrence of the short circuit inherent to the topology, and no need for additional isolation stages.

Based on the information mentioned, the development of this doctoral thesis to prove the technical feasibility and lower construction cost of the proposed converter compared to classic topologies found in the literature is based on the following structure:

- Comparative study between the most used multilevel converters;
- Presentation of the proposed new converter topology named SDC-CHB;
- Mapping and analysis of short-circuit states inherent to the proposed topology;
- Mathematical development of a STATCOM based on SDC-CHB as a power electronic device;
- Presentation of the predictive control concept and justification for the choice of OSV-MPC (Optimal Switching Vector - Model Predictive Control)
- Development of an SDC-CHB STATCOM control strategy based on OSV-MPC;
- Comparative simulations between SDC-CHB STATCOM and CHB STATCOM in Simulink Matlab® software;
- Implementation on the OPAL-RT 5700 hardware-in-the-loop platform for comparisons between SDC-CHB STATCOM and CHB STATCOM;
- Switching and conduction losses analysis of the STATCOM SDC-CHB based on MPC through PLECS® Plexim software.
- Conclusions about the proposed topology.

1.3 Thesis Outline

The subsequent chapters of this doctoral thesis are organized as follows:

Chapter 2 briefly presents the state of the art of the main multilevel converters used today and the SDC-CHB topology proposed in this work, highlighting their constructive aspects. A comparison between the listed topologies will also be presented.

Chapter 3 shows in detail the SDC-CHB topology and shows the short-circuit problems inherent in such a proposal. Mapping based on graph theory.

Chapter 4 presents the predictive control theory, with some most used strategies and their main characteristics. Mathematical modeling of the SDC-CHB STATCOM is developed to be controlled via OSV-MPC.

Chapter 5 presents the simulations of SDC-CHB STATCOM and CHB STATCOM in Simulink Matlab® software and their implementations on a hardware-in-the-loop (HIL) real-time platform from the manufacturer OPAL-RT, model 5700, to prove its applicability. Comparisons are made between the resulting signals obtained.

Chapter 6 presents the measurement and analysis of switching and conductivity losses of the MPC-based SDC-CHB STATCOM through the PLECS® Plexim software, where it is possible to observe the topology performance and its behavior concerning changes in the required load.

Chapter 7 exhibits the thesis conclusion and some recommendations and suggestions for future work.

Chapter 2: Multilevel Topologies

There are several multilevel converter topologies available in the literature. Some are more used in medium voltage applications, such as the diode-clamped multilevel converter (DCMC) [3, 24], the capacitor-clamped multilevel converter (CCMC) [3, 25], the modular multilevel converter (MMC) [3, 26, 27, 28] and the cascaded H bridge converter (CHB) [3, 29, 30, 31]. Each of them has important characteristics for this work, being exposed in this chapter.

2.1 Multilevel Topologies Presentation

2.1.1 Diode-Clamped Multilevel Converter

Over the past decades, in the commercial field, diode-clamped converters with three voltage levels prevailed in medium voltage applications. However, when required in high-power applications, this type of converter requires an increase in output voltage levels. In practice, the use of DCMC with more than three output voltage levels results in unbalanced capacitor voltages in DC-links, requiring additional DC-DC converters to regulate these voltages [24, 32, 33].

In high-power applications, which is necessary to increase the number of converter output voltage levels, the total components used in the arrangement will also grow as expected. In general, the DCMC of m voltage levels is composed of $2 \cdot (m-1)$ semiconductor switches, $2 \cdot (m-1)$ antiparallel diodes, $(m-1)$ capacitors, and $(m-1) \cdot (m-2)$ clamping diodes [34, 35].

With voltage levels addition, the number of power switches used in the converter increases linearly. However, the number of clamping diodes in the equipment increases almost quadratically, making the implementation of a DCMC with many voltage levels unfeasible. The excessive increase in the number of diodes in this topology is necessary due to the different limits of blocking the reverse voltage of the clamping diodes [24, 34, 35]. Figure 2-1 illustrates the growth in the number of components of a DCMC from 3 to 7 levels.

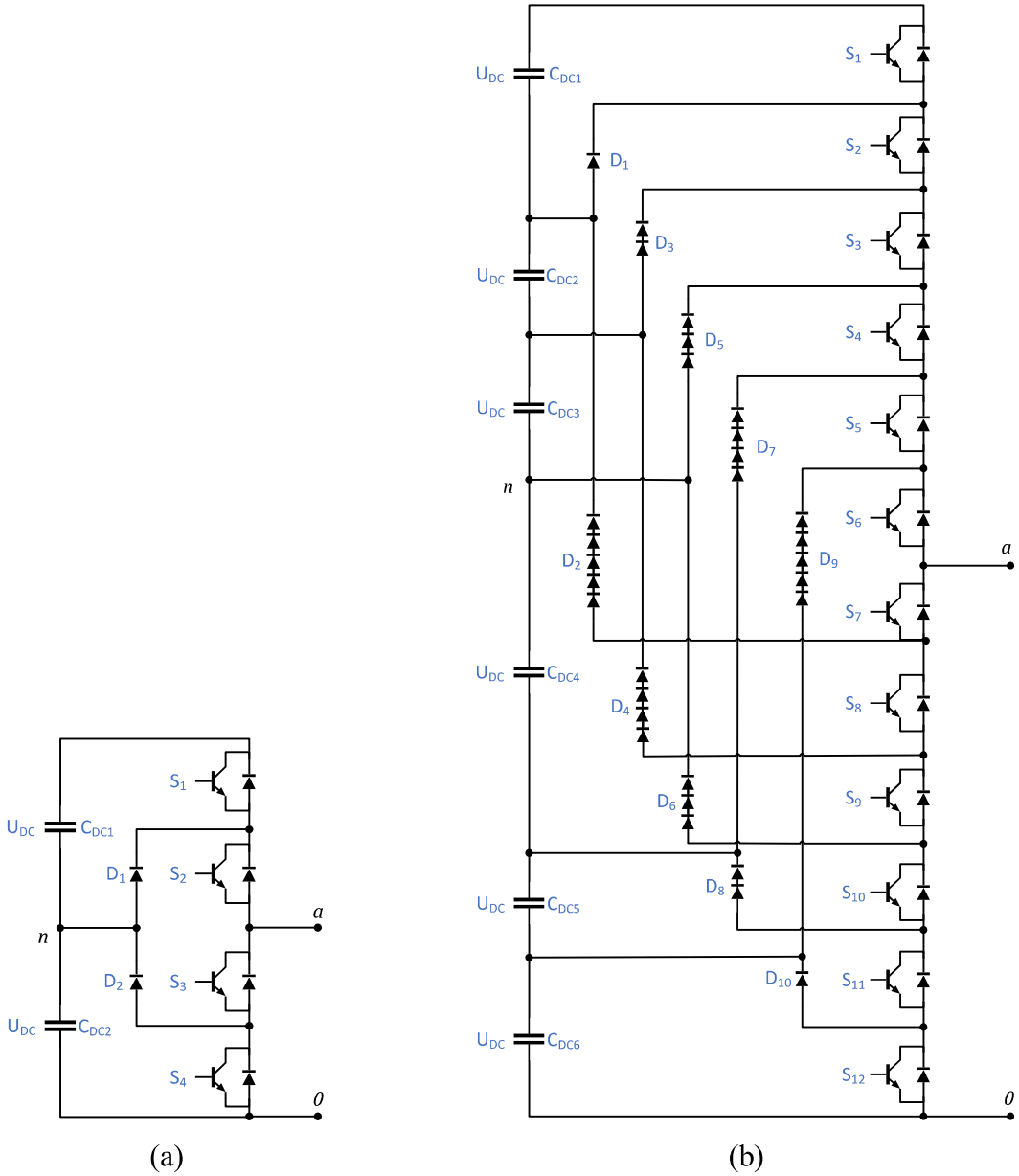


Figure 2-1– Contrast between the number of components of (a) a three-level DCMC and (b) a seven-level DCMC [24, 34, 35].

2.1.2 Capacitor-Clamped Multilevel Converter

Commonly known as flying-capacitor topology, the capacitor-clamped multilevel converters (CCMC) were first proposed by Meynard and Foch in 1992 as an alternative to diode-clamped converters [25, 36]. As a consequence, both topologies have several common advantages and disadvantages.

As with DCMC, increasing the number of voltage levels increases the number of its components. Therefore, a CCMC with m voltage levels is composed of $2 \cdot (m-1)$

semiconductor switches, $2 \cdot (m-1)$ antiparallel diodes, $(m-1)$ DC-link capacitors and $\frac{(m-1)\cdot(m-2)}{2}$ flying-voltage capacitors [32].

The capacitor-clamped multilevel converter also has an obstacle in the number of capacitors with the increment in the number of voltage levels, however, in a smaller proportion than the DCMC [33, 34, 36, 37, 38]. Thus, the number of power devices and capacitors of the DC-link (C_{DCn}, where n is the capacitor index) progresses linearly with the addition of output levels. However, for flying-voltage capacitors (C_n), their quantity increases almost quadratically [34, 35]. Figure 2-2 illustrates the increase in the number of components of a capacitor-clamped multilevel converter from 3 to 7 levels.

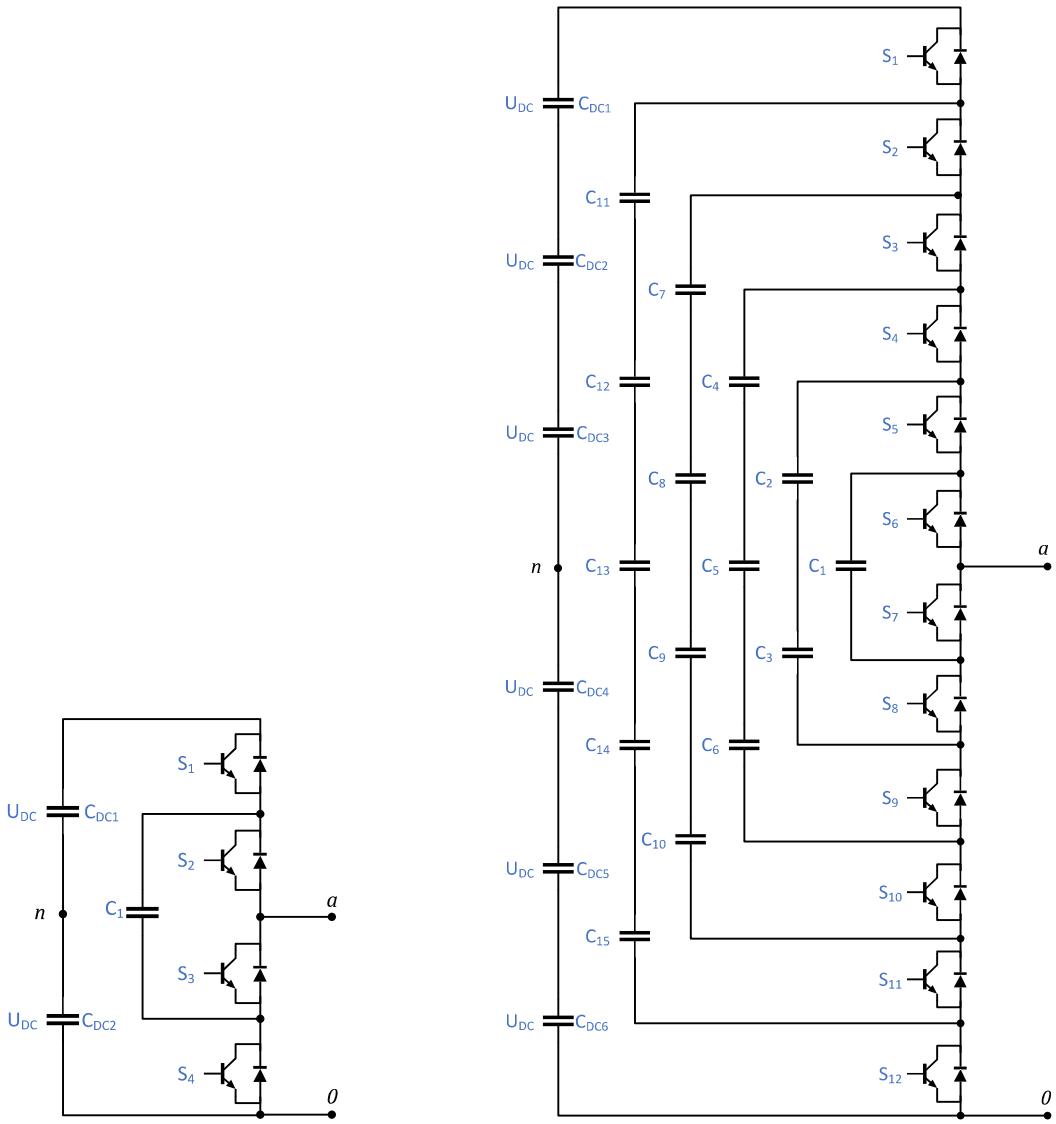


Figure 2-2– Contrast between the number of components of (a) a three-level CCMC and (b) a seven-level CCMC [36, 34, 35]

2.1.3 Modular Multilevel Converter (chopper cells) and Cascaded H bridge Converter

Due to the deregulation of international energy markets and the need for decentralized energy generation, the demand for advanced power electronics systems has grown consistently. For this branch of applications, modular converters appear as viable solutions due to the combination of semiconductor switch connections in series with the low harmonic distortion produced and mainly by modularization, which can be expandable, in theory, to any number of levels [34, 39]. For the sake of modular philosophy and the possibility of being scalable, the addition of central components (connecting the modules as in the DCMC and CCMC) should be avoided.

Among the multilevel modular topologies, MMC stands out using chopper cells [3, 26, 27] and CHB [3, 29, 30] using H bridge modules. Thus, both MMC and CHB are presented as converter topologies that can achieve high power and voltage levels without the use of coupling transformers, presenting a single-phase structure based on independent cells that, theoretically, do not have modularization limits [40].

However, the most significant differences between these two configurations refer to the number of modules in the MMC topology, which in the double star configuration has twice those in the CHB. However, the number of switches in these chopper cells is half of that in the H bridge cascade converter, resulting in the same number of semiconductor switches. The number of components is slightly higher in the MMC with chopper cells, thus having twice as many capacitors as the DC-link.

The most crucial advantage of CHB over MMC and other topologies of multilevel converters is the modest growth in the number of components about the other topologies showed, which presents a more relevant increase in the number of components in voltage levels. In this way, the number of circuit components is increased linearly with the number of levels desired at the converter output.

A double star chopper MMC with m voltage levels is composed of $2 \cdot (m-1)$ semiconductor switches, $2 \cdot (m-1)$ main diodes and $(m-1)$ DC-link capacitors [34, 35], while a CHB with m voltage levels is composed of $2 \cdot (m-1)$ semiconductor switches, $2 \cdot (m-1)$ main diodes and $\frac{(m-1)}{2}$ DC-link capacitors [35]. Despite the great advantages, this arrangement is not usually used in low-power applications [38].

Figure 2-3 illustrates the comparison between MMC structures of three levels (a) and seven levels (b) using chopper cells. Figure 2-4 presents the same comparison, but between a three-level CHB (a) and a seven-level CHB (b), using H bridge cells.

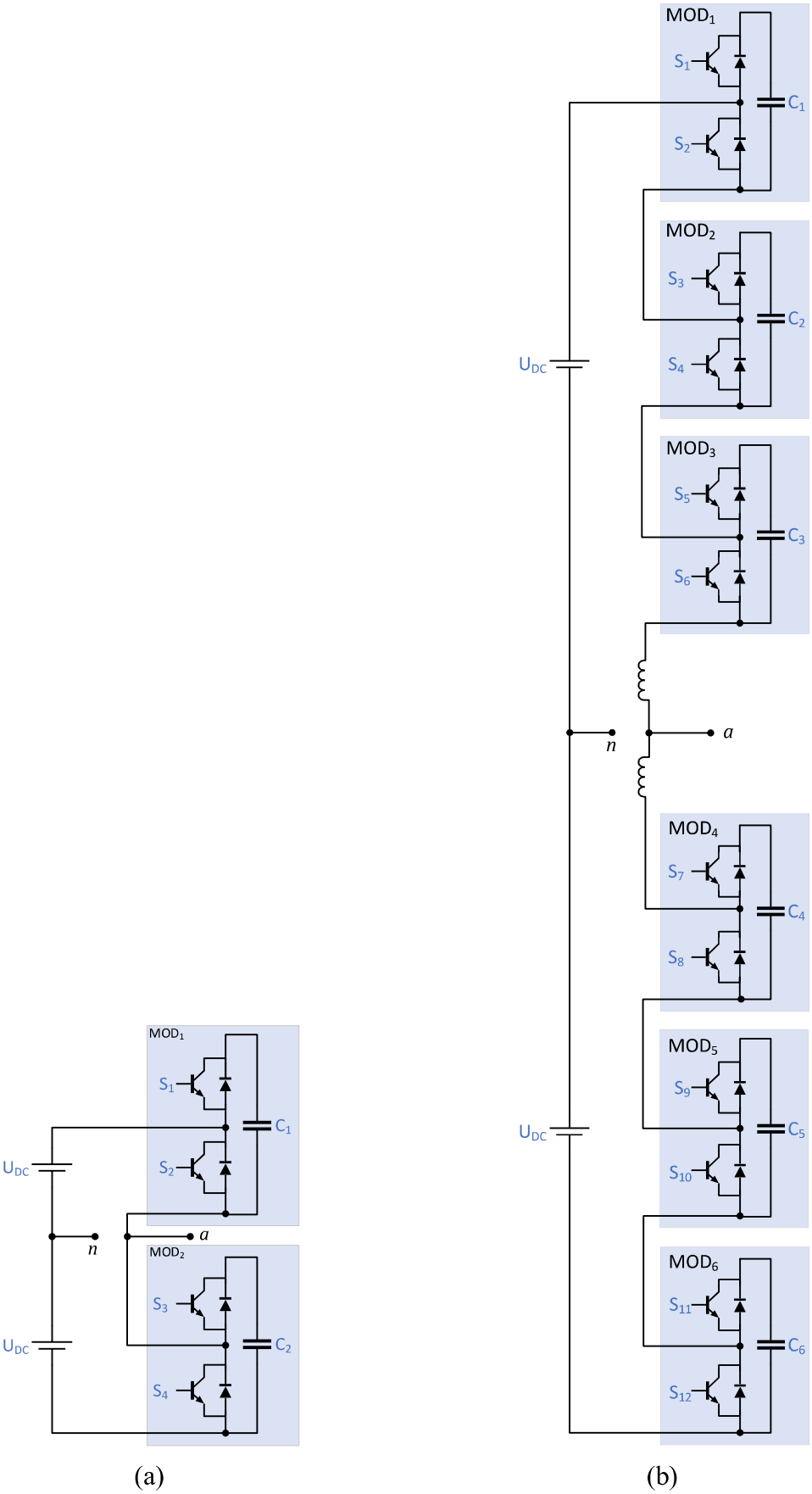


Figure 2-3– Contrast between the number of components of (a) a three-level MMC and (b) a seven-level MMC [3, 26, 27]

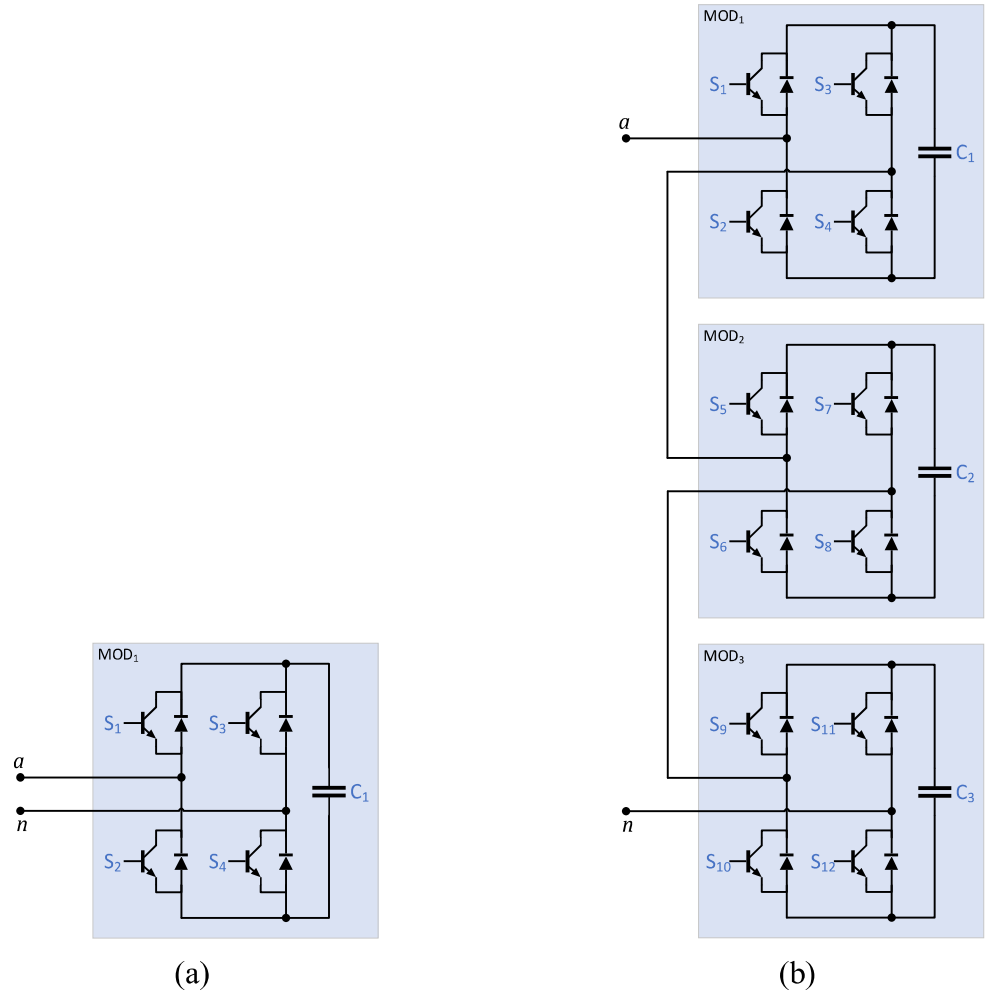


Figure 2-4– Contrast between the number of components of (a) a three-level CHB and (b) a seven-level CHB [3, 29, 30]

It should be noted that just the MMC has a DC bus.

2.1.4 Mixed-level Hybrid Multilevel Cells Converter

To comply with the requirements mentioned above, one of the prerequisites is that the converter must only be composed of identical modules. As demonstrated in 2.1.1 and 2.1.2, the DCMC and CCMC topologies have an almost exponential relationship between the output voltage levels and the number of components required by the converts, and this ratio is due to the DCMC and CCMC topologies non-modularity structure, requiring a high ratio of diodes and capacitors, respectively. Thus, some authors [29, 41, 42, 43, 44] proposed structure modifications to incorporate modularity in the DCMC and CCMC topologies. These alterations present a mixed-level hybrid multilevel cell (MHMC) using three-level single-phase DCMC or CCMC cells to compose multilevel converters (MHMC DCMC and MHMC CCMC) with more voltage levels.

By adopting DCMC or CCMC cells to replace full-bridge cells, the number of independent DC sources is also reduced, and as a consequence, the voltage level is doubled in each cell. In this way, only two cells connected in cascade are necessary to achieve a converter with nine voltage levels and add modular characteristics. Figure 2-5 shows nine-level converters based on three-level CCMC cells (a) and DCMC cells (b). If necessary, a capacitor-clamped cell can be replaced by another cell based on the diode-clamped, or vice versa, this being the origin of the hybrid nomenclature [29].

Therefore, an MHMC-CCMC with m voltage levels is composed of $4 \cdot (m-1)$ semiconductor switches, $4 \cdot (m-1)$ antiparallel diodes, $(m-1)$ DC-link capacitors, and $(m-1)$ flying-voltage capacitors, and an MHMC-DCMC with m voltage levels is composed of $4 \cdot (m-1)$ semiconductor switches, $4 \cdot (m-1)$ antiparallel diodes, $(m-1)$ DC-link capacitors, and $2 \cdot (m-1)$ clamped diodes.

There are also the asymmetric hybrid multilevel cells (AHMC) topology [29, 41] that propose a moderate growth in the components required versus voltage levels. Besides, some cells can work with high switching frequency and others with low frequency due to the difference in voltage level. The lower frequency cells typically operate at the fundamental frequency while the upper cells use high frequency, thus smoothing out the final waveform. However, the AHMC topology does not have modular characteristics and presents a very complex DC-link capacitor voltage control due to the different DC voltage values [41].

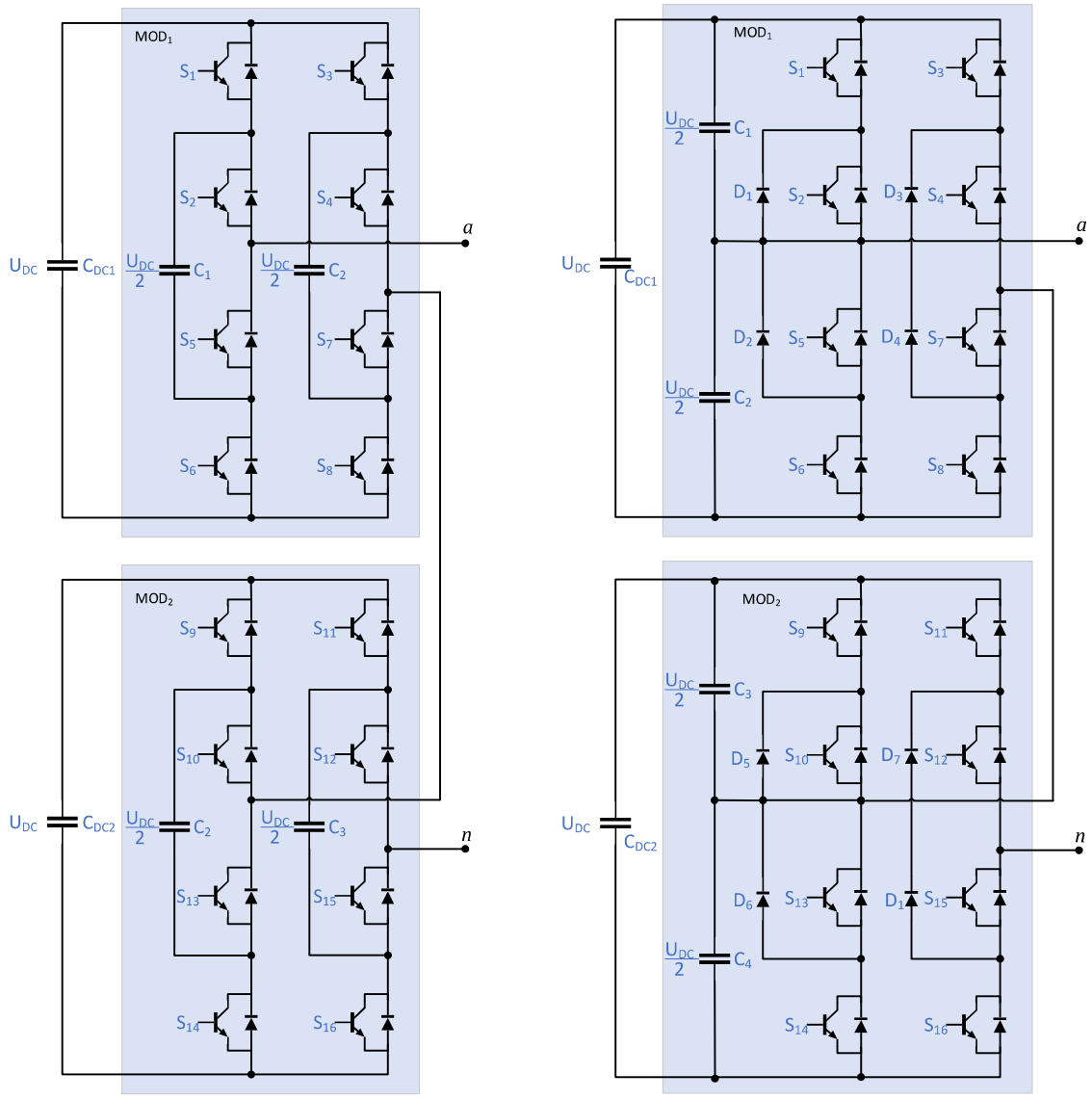


Figure 2-5– Comparison between (a) a nine-level MHMC-CCMC, and (b) a nine-level MHMC-DCMC [29, 41]

2.1.5 Cascaded H Bridge Converter with Single DC-link (proposed topology)

The topologies of multilevel converters presented in sections 2.1.1 to 2.1.4 are widely known, being the object of several studies in the literature. However, these topologies have single-phase structural characteristics, that is, they use DC-links, connected in series or not, which relate only to one phase, just replicating the same single-phase structure two more times to obtain a three-phase converter.

In addition to needing more constructive components, the other topologies, when operating in three-phase converters, present oscillations of twice the fundamental frequency

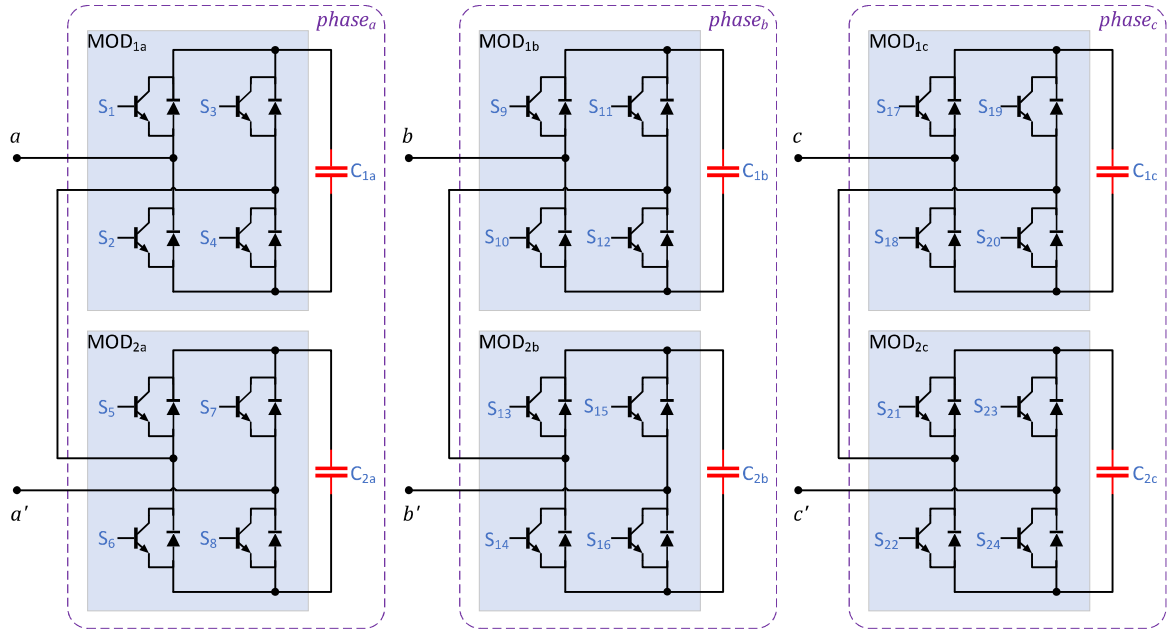
(2ω) in the DC link, being notable characteristics in single-phase systems [11]. These oscillations are due to the need to obtain constant values on the DC-links while the power flow pulsates in single-phase structures.

From the perspective of high-power applications, modularity, and moderate growth of components, the CHB topology based on H bridge cells becomes an effective and viable option for electronics applied to power converters.

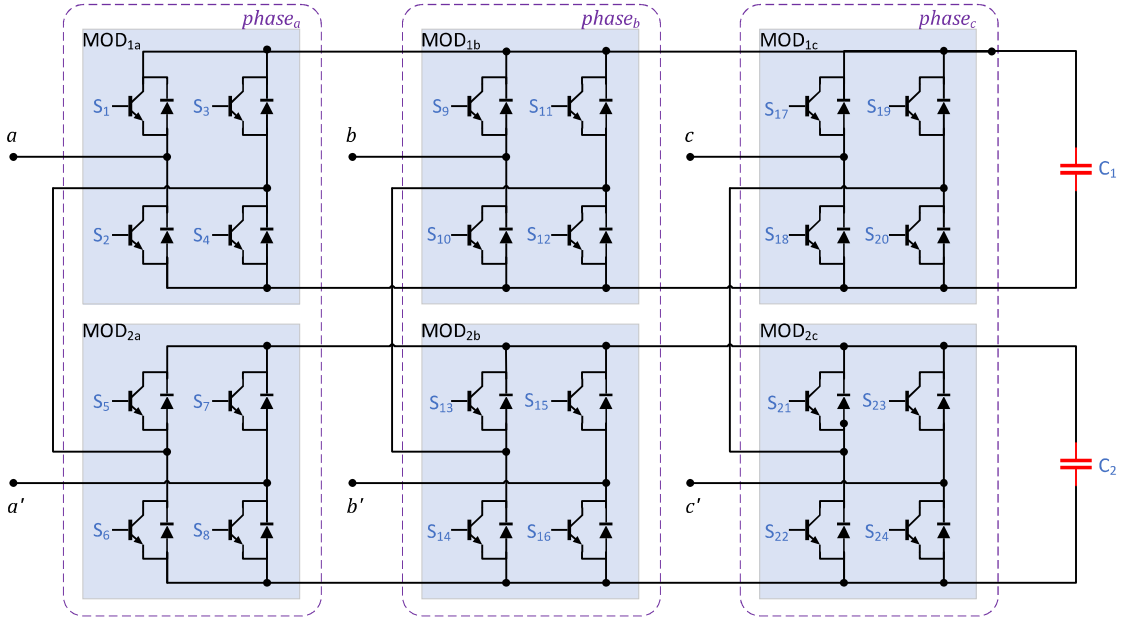
Therefore, to propose an upgrade to the classical CHB structure, this work suggests a new power converter topology that can be used in a wide variety of applications. This proposed topology, in addition to having modular characteristics, also uses H bridge cells, like the single-phase based CHB, utilizing, however, a three-phase DC-link structure, employing three times fewer capacitors when compared to the conventional single-phase CHB topology [7, 11]. Furthermore, this topology is also free from the low-frequency DC-link energy oscillation typical from single-phase converters.

The CHB classical multilevel structure and the SDC-CHB topology are shown in Figure 2-6 (a) and (b), respectively, where their H bridge structures can be observed, as well as its modular attributes, which is essential for defective cell replacement [45, 46], and also for a future expansion of its quantity, for example [47, 48]. The main constructive difference between the compared topologies is the capacitor connections and the DC-links designing, which have a single-phase structure in the traditional CHB and a three-phase structure in the SDC-CHB topology [11].

It is noteworthy that DC-links shared between the phases do not affect the modularity of the topology since it is possible to use H-bridge cells with their capacitors as long as they are connected in parallel with each other. The advantage of this type of connection concerning a single capacitor for the three phases is the marked reduction in the capacitance value and better fault tolerance, facilitating the replacement of defective modules.



(a)



(b)

Figure 2-6– Structural comparison between three-phase topologies: (a) classical multilevel CHB topology; (b) proposed SDC-CHB topology [7, 11].

Therefore, an SDC-CHB with m voltage levels is composed of $6 \cdot (m-1)$ semiconductor switches, $6 \cdot (m-1)$ main diodes, and $\frac{(m-1)}{2}$ DC-link capacitors.

However, despite the constructive simplicity, fewer structural components, and the DC-link voltage oscillation mitigation, SDC-CHB provides many short-circuit states if a switching strategy based on pulse width modulation is used [49]. This condition makes this

topology unfeasible when used with these classic switching strategies [11]. The short-circuit states analysis of the proposed topology will be presented and developed in Chapter 3.

2.2 Comparison Between Multilevel Topologies

After being exposed to the significant characteristics of the different topologies of existing multilevel converters, it can be observed that only the CHB, MMC, and MHCM have modular structures, allowing additional cell series connection. Furthermore, the SDC-CHB topology stands out with fewer components than other topologies, as shown in Figure 2-7, which is based on Table 2-1. It should be noted that the SDC-CHB topology has a three-phase structure. Therefore, most of the values related to the components of the other topologies, which have a single-phase structure, are multiplied by three.

Table 2-1 - Number of components for each multilevel topology.

Topology	Semicondutor Switches	DC-link Capacitors	Flying-Capacitors	Antiparallel Diodes	Clamping-Diodes
DCMC	$3 \cdot 2 \cdot (m-1)$	$(m-1)$	0	$3 \cdot 2 \cdot (m-1)$	$3 \cdot (m-1) \cdot (m-2)$
CCMC	$3 \cdot 2 \cdot (m-1)$	$(m-1)$	$\frac{(m-1) \cdot (m-2)}{2}$	$3 \cdot 2 \cdot (m-1)$	0
MHMC (DCMC)	$3 \cdot 4 \cdot (m-1)$	$3 \cdot (m-1)$	0	$3 \cdot 4 \cdot (m-1)$	$3 \cdot 2 \cdot (m-1)$
MHMC (CCMC)	$3 \cdot 4 \cdot (m-1)$	$3 \cdot (m-1)$	$3 \cdot (m-1)$	$3 \cdot 4 \cdot (m-1)$	0
MMC	$3 \cdot 2 \cdot (m-1)$	$3 \cdot (m-1)$	0	$3 \cdot 2 \cdot (m-1)$	0
CHB	$3 \cdot 2 \cdot (m-1)$	$\frac{3 \cdot (m-1)}{2}$	0	$3 \cdot 2 \cdot (m-1)$	0
SDC-CHB	$3 \cdot 2 \cdot (m-1)$	$\frac{(m-1)}{2}$	0	$3 \cdot 2 \cdot (m-1)$	0

The evolution of the number of components with the increase in the voltage levels is noted in Figure 2-7. It can be seen intense growth, mainly in non-modular topologies (DCMC and CCMC). The hybrid MHMC topologies have a more moderate increase but present values substantially higher than those observed in the MMC, CHB, and SDC-CHB topologies. However, the latter presents the best relationship illustrated in the graph.

Another advantage of the SDC-CHB, among the topologies that present 2ω oscillations, is the only modular topology.

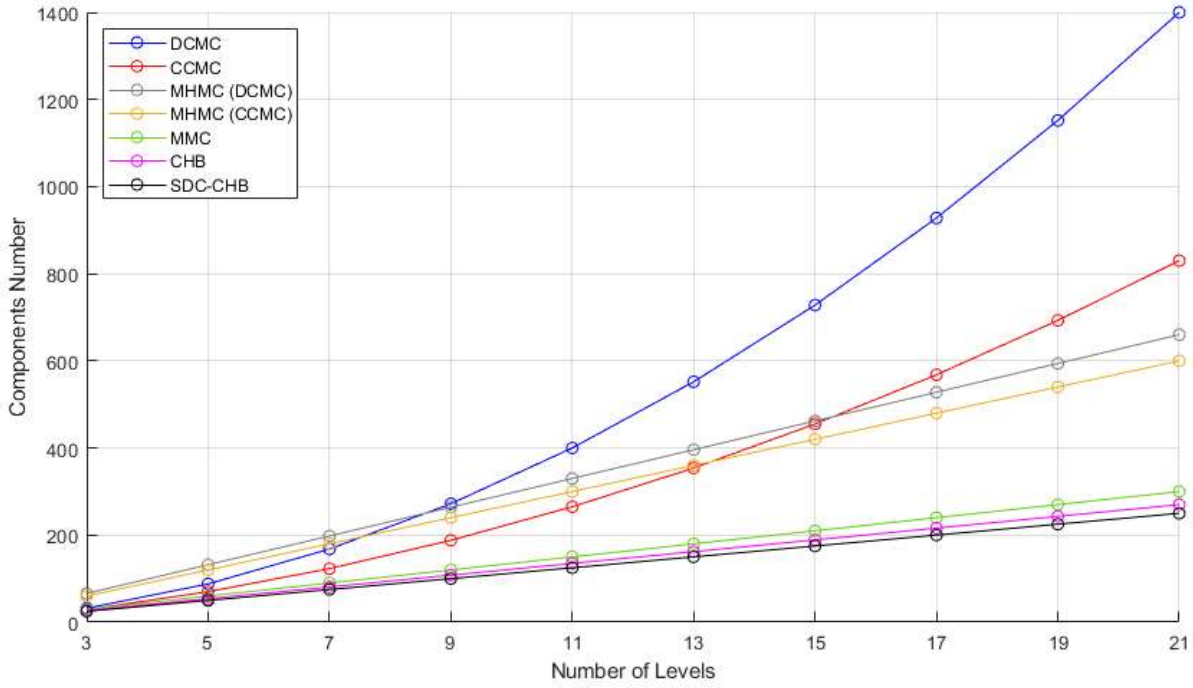


Figure 2-7– Elements quantities comparison required for each multilevel converter according to the number of levels [7, 11]

Lastly, the proposed topology is based on a full-bridge converter ensuring a unitary ratio between the single-phase peak voltage and the DC-link voltage. Most converters, except CHB, consist of a half-bridge converter, maintaining only a 50% ratio between the output voltage and the DC-link voltage. Table 2-2 summarizes the comparison of the multilevel converters.

Table 2-2 - Comparison between multilevel topologies.

Topology	**Components Number**	**Modularity**	**2ω Oscillation**	$\boldsymbol{Full-Bridge}$
DCMC	very high	no	no	no
CCMC	high	no	no	no
MHMC (DCMC)	high	yes	yes	no
MHMC (CCMC)	high	yes	yes	no
MMC	low	yes	yes	no
CHB	low	yes	yes	yes
SDC-CHB	very low	yes	no	yes

Thus, it can be concluded that the SDC-CHB structure is the only one that presents simultaneously:

- low evolution in the number of the components, reducing the cost of construction and its implementation;
- modularity, allowing the replacement of defective modules with another of the exact specifications, facilitating their maintenance and improving their fault tolerance;
- absence of 2ω oscillation on the capacitors DC-link, presenting more constant voltages and facilitating their control;
- Reduction of the total capacitance required by the converter;
- structure based on full-bridge converters, improving the current pattern and control of the DC-link voltages.

Chapter 3: The SDC-CHB Analysis

This chapter presents the main advantages of SDC-CHB topology over the classic CHB as well as an analysis of short-circuit states in the new proposal.

3.1 The SDC-CHB Topology

As previously mentioned, this thesis suggests a new power converter topology, employing three times fewer capacitors than classic CHB due to its three-phase structure, thus, reducing the total converter cost and reducing the DC-link voltage control complexity [11].

The CHB classical multilevel structure and the SDC-CHB topology are shown in Figure 2-6 (a) and (b), respectively, where its H bridge structures can be observed, as well as its modular attributes, which is essential for defective cell replacement [45, 46], and also for a future expansion of its quantity, for example [47, 48]. The main constructive difference between the compared topologies is the capacitor connections and the DC-links designing, which have a single-phase structure in the traditional CHB and a three-phase structure in the SDC-CHB topology [11].

3.1.1 The SDC-CHB Capacitance

Regarding the capacitors necessary to produce the appropriate DC-link ripple values, the SDC-CHB structure, in addition to presenting a smaller capacitors number concerning single-phase structures, present total capacitance values, on average, six times lower than the classical CHB topology [49, 50, 51, 52, 53]. Some studies claim that these values can be up to ten times lower [45, 54, 55, 56], demonstrating the evident superiority of three-phase structures over single-phase structures in terms of the total capacitance.

The equations (1) [49] and (2) [45] used in this work represent the total capacitance for the CHB and the SDC-CHB, respectively.

$$C_{CHB} = \frac{P}{\omega \cdot U_{DC} \cdot \Delta U} \quad (1)$$

$$C_{SDC-CHB} = \left(\frac{1}{10}\right)\frac{P}{\omega \cdot U_{DC} \cdot \Delta U} \quad (2)$$

Where C_{CHB} and $C_{SDC-CHB}$ are the total CHB and SDC-CHB capacitance, respectively; S is the total converter power; ω the grid angular frequency; U_{DC} is the DC-link voltage average; and ΔU is the DC-link voltage ripple.

It is essential to highlight that the values obtained by (1) and (2) represent the total converter capacitance values[1]. That is, even though SDC-CHB has three times fewer capacitors, it has ten times less total capacitance used than the classic CHB for the same voltage ripple values design.

That is, considering:

$$C_{CHB} = 10 \cdot C_{\mathrm{SDC-CHB}}$$
$$N_{CHB} = 3 \cdot N_{SDC-CHB}$$

Where N_{CHB} and $N_{SDC-CHB}$ are the CHB and SDC-CHB amount of capacitors, respectively, the values of individual capacitors in both topologies are expressed by equations (3) and (4):

$$C_{iSDC-CHB} = \frac{C_{SDC-CHB}}{N_{SDC-CHB}} \quad (3)$$

$$C_{iCHB} = \frac{C_{CHB}}{N_{CHB}} = \frac{10 \cdot C_{SDC-CHB}}{3 \cdot N_{SDC-CHB}} = \left(\frac{10}{3}\right)\frac{C_{3\emptyset}}{N_{SDC-CHB}} = \left(\frac{10}{3}\right)C_{iSDC-CHB} \quad (4)$$

Where $C_{iSDC-CHB}$ and C_{iCHB} are the SDC-CHB individual capacitor value and CHB individual capacitor value, respectively.

That is, for a given DC-link ripple value, not only does the CHB structure has three times more capacitors than the SDC-CHB structure, but each CHB individual capacitor will have a capacitance value $^{10}/_{3}$ times greater than the SDC-CHB individual capacitor, which increases the equipment cost and volume.

[1] Equivalent to the sum of all converter capacitances for capacitors cost purposes.

3.2 Converter Short-Circuit States Analysis

For the SDC-CHB short-circuit analysis, a five-level phase voltage output converter was chosen, as presented in Figure 2-6 (b), which can be connected directly to the grid or a load or through a transformer. SDC-CHB has some switching states in which one or both capacitors are short-circuited, which could damage the converter [11], as shown in Figure 3-1. Since these failures occur in several switching states, these converters cannot be used without an additional stage capable of avoiding their natural short circuits using PWM (Pulse Width Modulation) strategies, for example [49, 57].

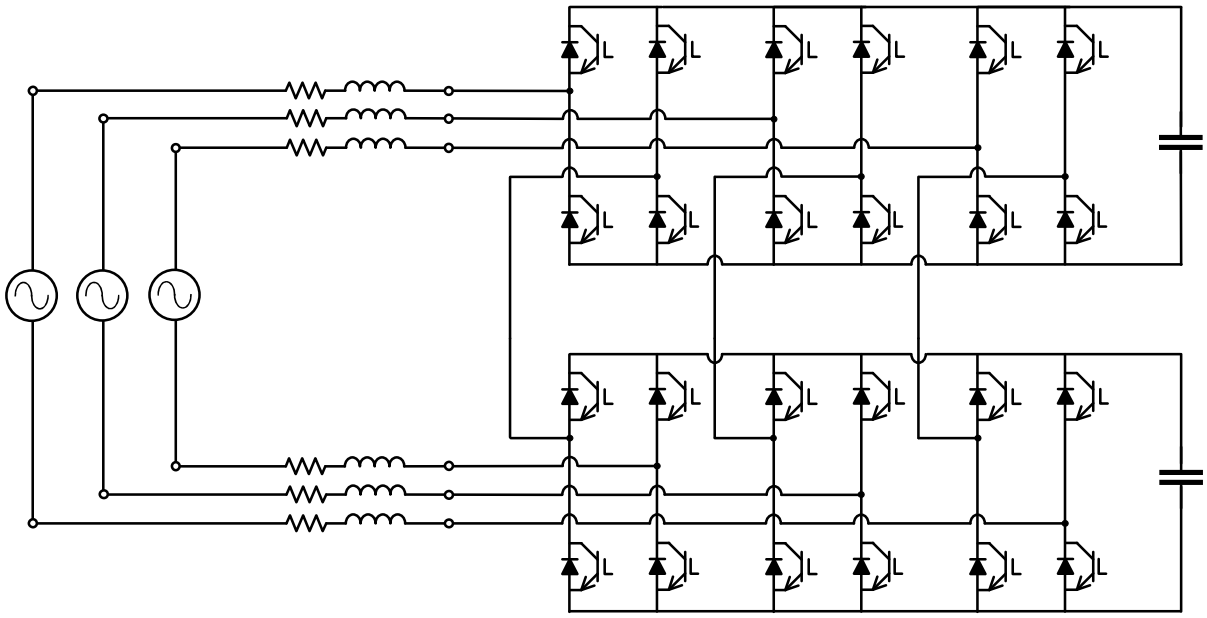
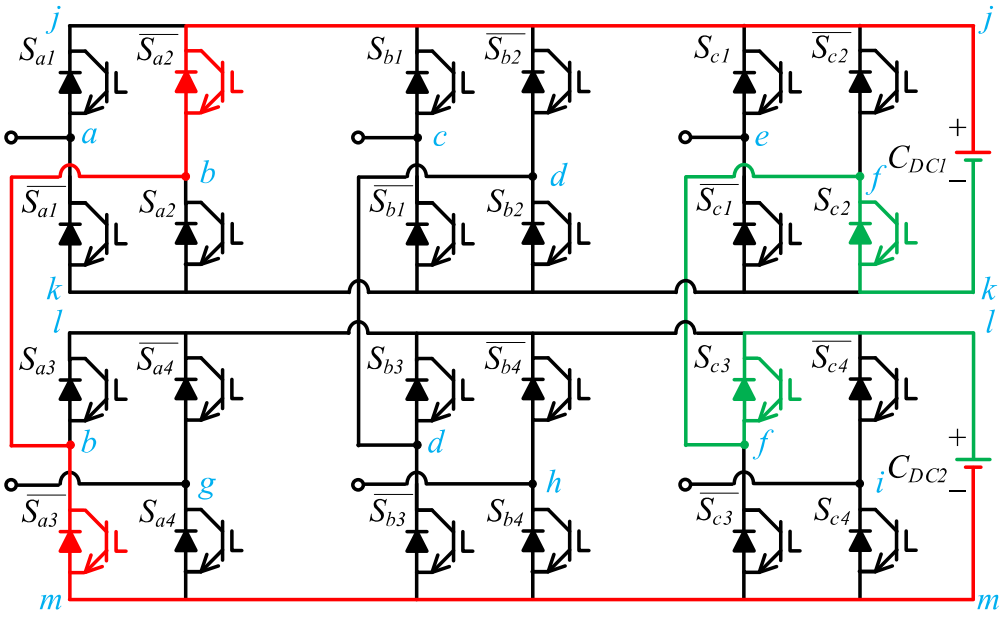


Figure 3-1– Example of SDC-CHB application through a direct connection.

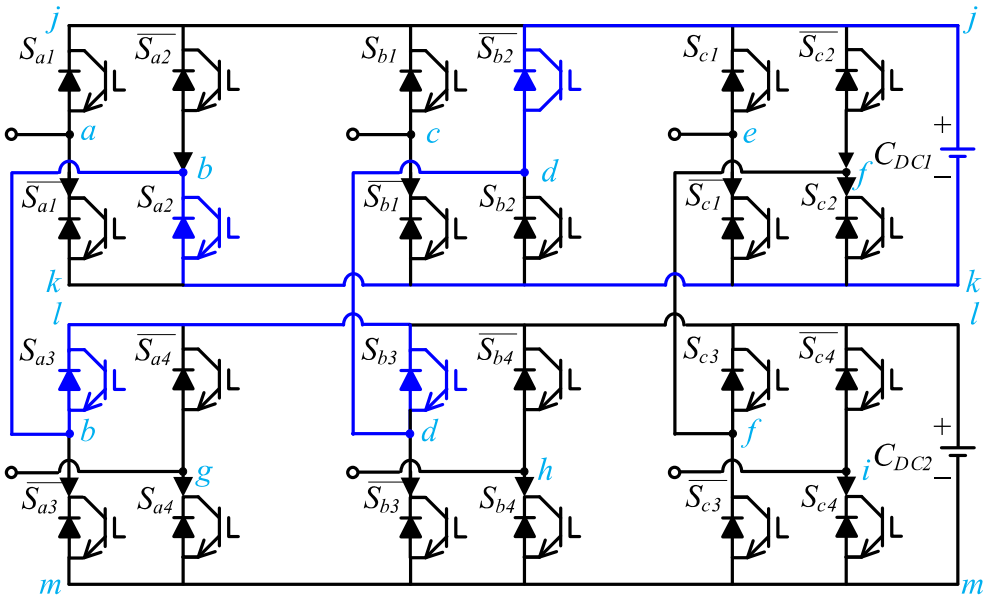
The effective methodology development capable of mapping the prohibitive states becomes an important barrier to be overcome during studies about the short-circuit stages inherent to this converter. Therefore, a path analysis taken by the electric current in each different state combination of each converter switch is necessary. These conditions are illustrated in Figure 3-2, where each of the 24 semiconductor switches in this topology has two possible states (ON or OFF), being possible 2^{24}, that is, 16,777,216 different switching states. Some of the many prohibited states identified are highlighted: in red and green in Figure 3-2 (a), where both capacitors (C_{DC1} and C_{DC2}) are short-circuited; in blue in Figure 3-2 (b), where C_{DC1} capacitor is short-circuited; and in yellow in Figure 3-2 (c), where C_{DC2} capacitor is short-circuited.

However, the switches in the same H bridge module arm are interlocked. That is, the S_{a1} switch has an opposite state to the $\overline{S_{a1}}$ switch, for example. This strategy, with unipolar modulation characteristics, reduces the number of control signals and, as a result, reduces the different switching states' number, .

By this converter structural peculiarity virtue, it can be controlled with just 12 processed signals, referring to the S_{nm} switches (where $n = a, b, c$ and $m = 1,2,3,4$). Thus, the amount of possible combinations reduces to 2^{12}, that is, 4096 distinct states, sharply sparing the required processing capability.



(a)



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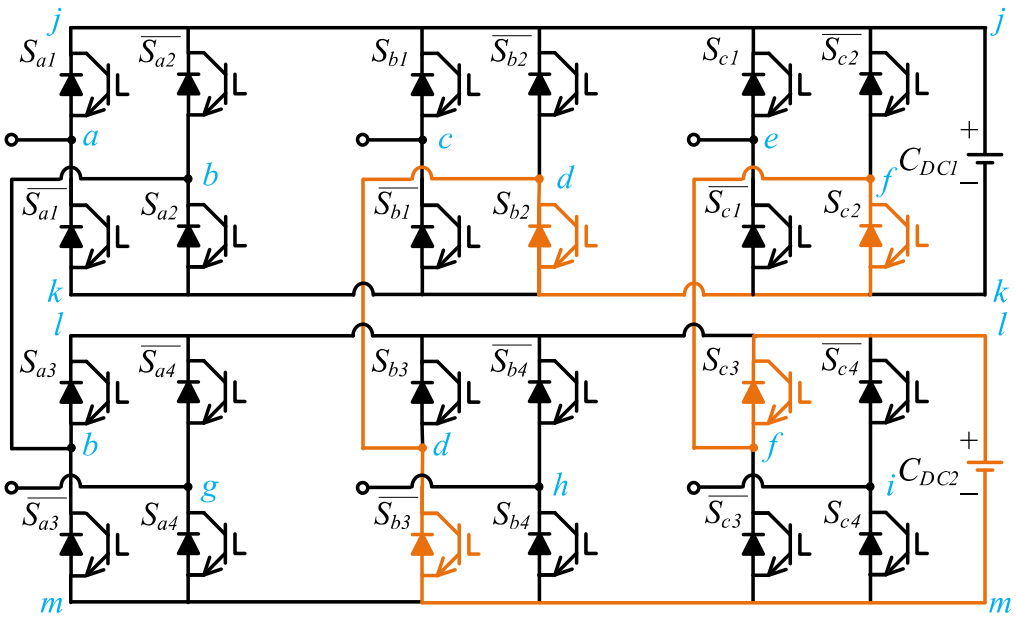


(c)

Figure 3-2– SDC-CHB short-circuits current path examples: (a) C_{DC1} and C_{DC2} in short-circuit [11]; (b) C_{DC1} in short-circuit; (c) C_{DC2} in short-circuit.

The graph theory was applied to map all possible converter switching states and identify each of its allowed or prohibited states. This theory consists of a mathematical branch intended to study relationships between objects of a given set, producing abstract graphic structures known as graphs.

> *"A graph $G(V, A)$ is defined by the pair of sets V and A, where: V is a non-empty set: the vertices or nodes of the graph; A is a set of pairs ordered, $a = (v, w), v$ and $w \in V$: the edges of the graph."* [58].

A graph is represented by a set of so-called vertices and their interdependent relations known as edges. In the case of the studied converter, each electrical node was classified as a vertex and each switch as an edge, thus allowing to trace all the existing electrical current paths.

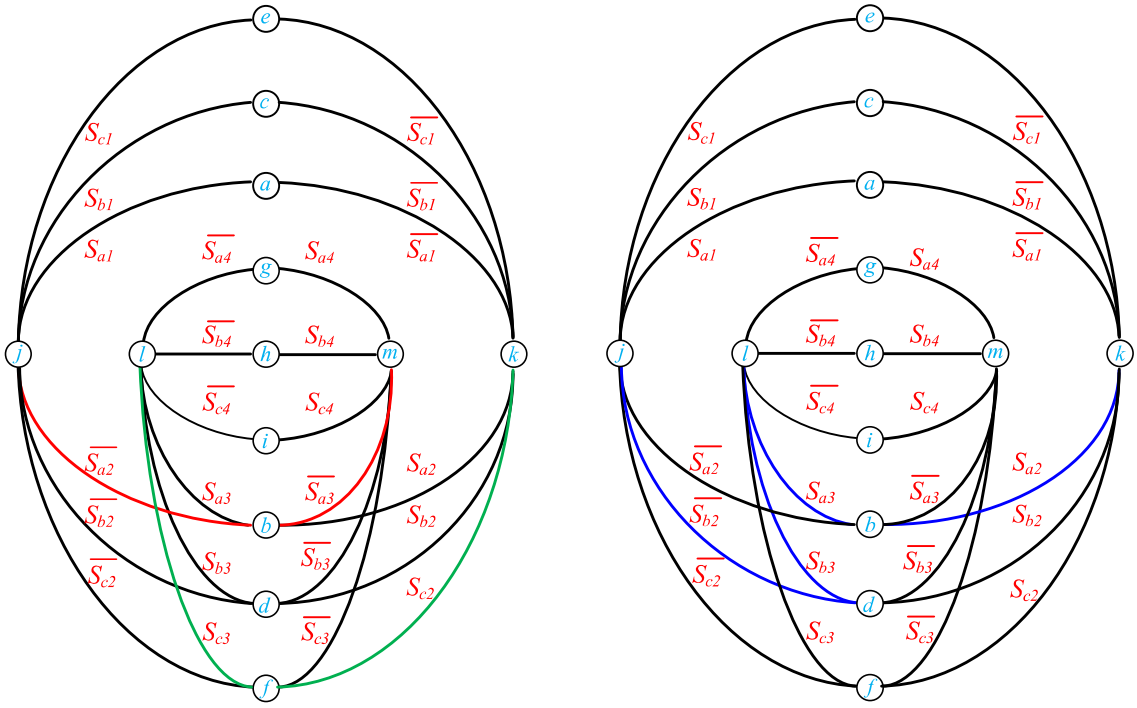
In this way, an algorithm is used that makes it possible to scan each of the connections between edges and vertex, identifying all switching combinations capable of connecting opposite poles of the same capacitor or of an adjacent capacitor, which electrically corresponds to the short-circuit states.

This methodology can be used in any power electronics converter, including those who have any number of modules like the modular converters, since such devices have well-determined switching states and electrical current paths.

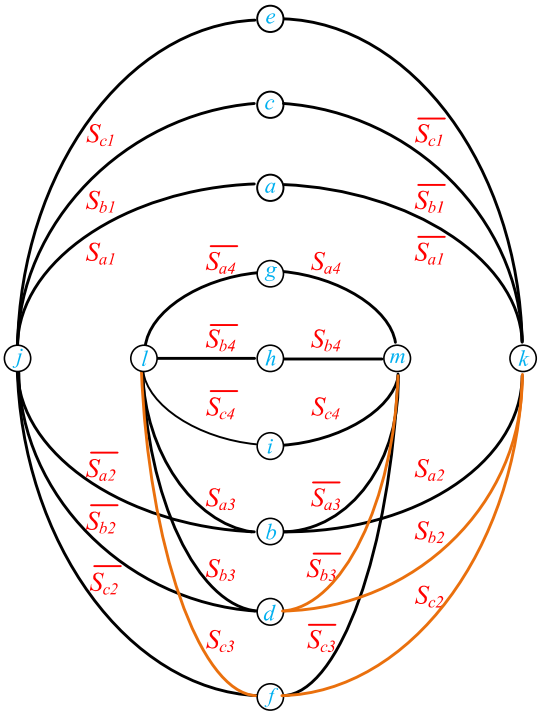
Graph theory can be applied to countless everyday situations, since it studies the combination of elements, being used mainly in the fields of computer science, mathematics, probability, psychology, engineering, among others.

For the problem of SDC-CHB short circuit states in question, brute force and individual actuation of the semiconductor switches can be used to analyze the measured currents, however, the graph theory presents a less costly and scientifically more elegant output, just adapt the algorithm to the project's characteristics.

The colored lines in Figure 3-3 correspond to the short circuits highlighted in Figure 3-2, and illustrates the converter graph, showing all possible SDC-CHB connections where can be observed the existence of three possible short circuits types: the first one with the C_{DC1} and C_{DC2} capacitors, simultaneously, in short-circuit, that is, with the j point connected to the m point and the k point connected to the l point, simultaneously; the second with the C_{DC1} capacitor in fault state, that is, with the j point connected to the k point; and, finally, the third, with the C_{DC2} capacitor in short-circuit, that is, with the l point connected to the m point.



(a) (b)



(c)

Figure 3-3– Graphs for SDC-CHB short-circuit states analysis: (a) C_{DC1} and C_{DC2} in short-circuit [11]; (b) C_{DC1} in short-circuit; (c) C_{DC2} in short-circuit [7].

Thus, with graph theory applied to this five-level converter, a computer algorithm was developed, capable of gathering each one of the 4096 possible paths and mapping the converter's unipolar switching states [11, 16, 22, 59, 7]. Only 640 states are useful out of the 4096 possible states. (less than 16% of combinations)

It can be observed in Table 3-1 that the 640 permissible switching states are mainly distributed among the voltage values per phase between $-U_{dc}, 0\ and\ +U_{dc}$, representing 95% of them. Although the vast majority of switching states represent prohibitive states, that is, short-circuit states, the converter can synthesize all five voltage levels per phase, as shown in Figure 3-4, where the red dots represent the possible three-phase vector voltage. This characteristic is essential for building a three-phase sinusoidal wave with low total harmonic distortion (THD), a fundamental condition for using the SDC-CHB in several power electronics equipment, as mentioned above.

Table 3-1 - Number of combinations per phase voltage.

Phase Voltage	Number of Combinations
$-2U_{dc}$	16
$-U_{dc}$	160
0	288
$+U_{dc}$	160
$+2U_{dc}$	16
Total	**640**

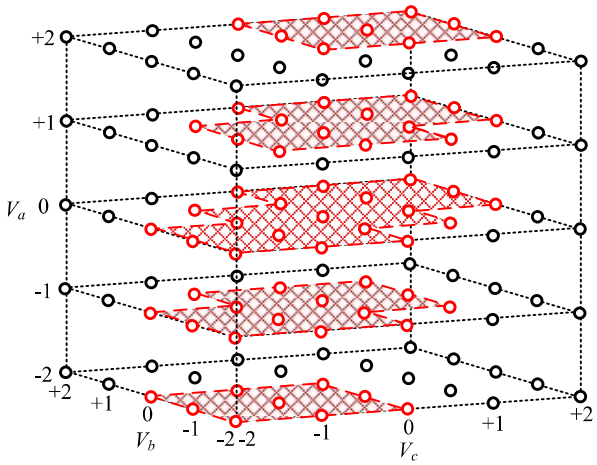


Figure 3-4– Possible voltage vectors per phase after restrictions [7, 11].

3.3 SDC-CHB STATCOM

Although there is the possibility of synthesizing all the required voltage levels, the low percentage of possible states makes this topology unfeasible in applications based on PWM modulation. The uncertainty about the exact moment and the exact combination of switches demanded by these strategies provide for each switching the 84% probability of choosing a prohibitive state. Thus, it is necessary to adopt a switching strategy particularly developed for each application of this converter.

To prove the applicability of the presented structure, its application as STATCOM in a three-phase grid is suggested to control the injection of reactive power according to the desired reference and shown in Figure 3-5. For that, a control based on MPC was developed, which makes it possible to use the allowed states of the converter, inhibiting short-circuit states and providing other inherent advantages of this strategy.

Inductors and resistors are used as a filter in the connection of the SDC-CHB with the power grid to adjust the harmonic distortion indices to the current regulations, as well as intra-module damping inductors to reduce the current peaks inherent in the switching of each module. The number of dumping inductors is represented by relation $3N - 1$, where N is the number of modules.

The following chapters present the concept of predictive control, its applicability to the proposed problem, and the results obtained from its implementation in two different software platforms.

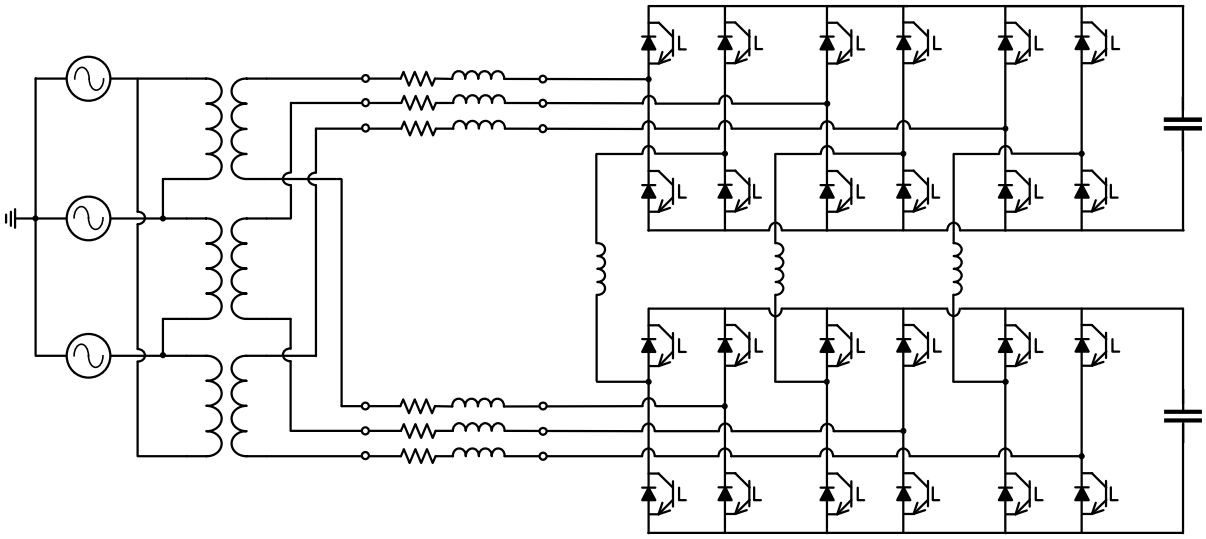


Figure 3-5– SDC-CHB STATCOM [7, 11].

Chapter 4: Model Predictive Control Applied to STATCOM

Model predictive control has been a research and development topic since the 1970s when it was initially introduced into the industry of processes [60, 61, 62, 63]. The MPC has a broad concept involving many areas. Its central concept is the prediction of the future states of the system, based on a mathematical model, given a time horizon. An optimized control action is then chosen to minimize the cost function, which is based on a reference and the predicted states. Usually, this function, also known as the cost function, is expressed as a quadratic relation of states and control signals. When minimized, the system's trajectory goes to the origin as in a quadratic linear regulator [64, 65]. As cost function optimization requires much computational effort, only from the 1990s [66], with the tremendous technological advance of microprocessors, this strategy was proposed and studied as a promising alternative for the control of energy converters and drives [67].

The use of the control in power electronics converters is restricted to the set of equipment possible switching states. Thus the MPC becomes a feasible option and with less implementation complexity [29, 62]. Furthermore, MPC-based strategies are intuitive, simple, and easy to implement, allows nonlinearities and constraints to be incorporated simply, and it is possible to group several loops in just one, in addition to the possibility of including penalties or other limitations [63, 68, 69].

An MPC controller has the following structure [69]: the use of a reliable model to predict the system states in future time instants; the calculation of a control sequence to minimize the cost function; at each time interval, only the first element of the control signal is applied to the process, and the time horizon is shifted to an instant of future time [64].

As the SDC-CHB structure proposed in this thesis is a power electronics topology, with known semiconductor switch states with limited quantity, in addition to having restrictions on the sequence of its drives, the MPC can be an attractive strategy for the operation of an SDC-CHB-based converter. To prove the applicability and viability of this structure, the main classes of MPC will be presented to better understand the choice of the strategy to be applied to the SDC-CHB STATCOM.

4.1 Predictive Control Classification

The main characteristic of predictive control is the use of a system model to predict the future behavior of the controlled variables, and based on these data, provide the controller with substantial material to obtain the best performance according to predefined optimization criteria [63].

A classification for some different predictive control methods is present in Figure 4-1 [70].

Briefly, the optimization method based on hysteresis consists of maintaining a specific control variable within the boundaries of the hysteresis area [63, 71]. In trajectory-based control, variables are forced to follow a predefined trajectory [63, 72]. In deadbeat control, the optimal performance makes the error equal to zero in the next sampling instant [63, 73, 74]. Finally, in the model predictive control (MPC), a more flexible criterion is used, presenting a cost function to be minimized [63, 62].

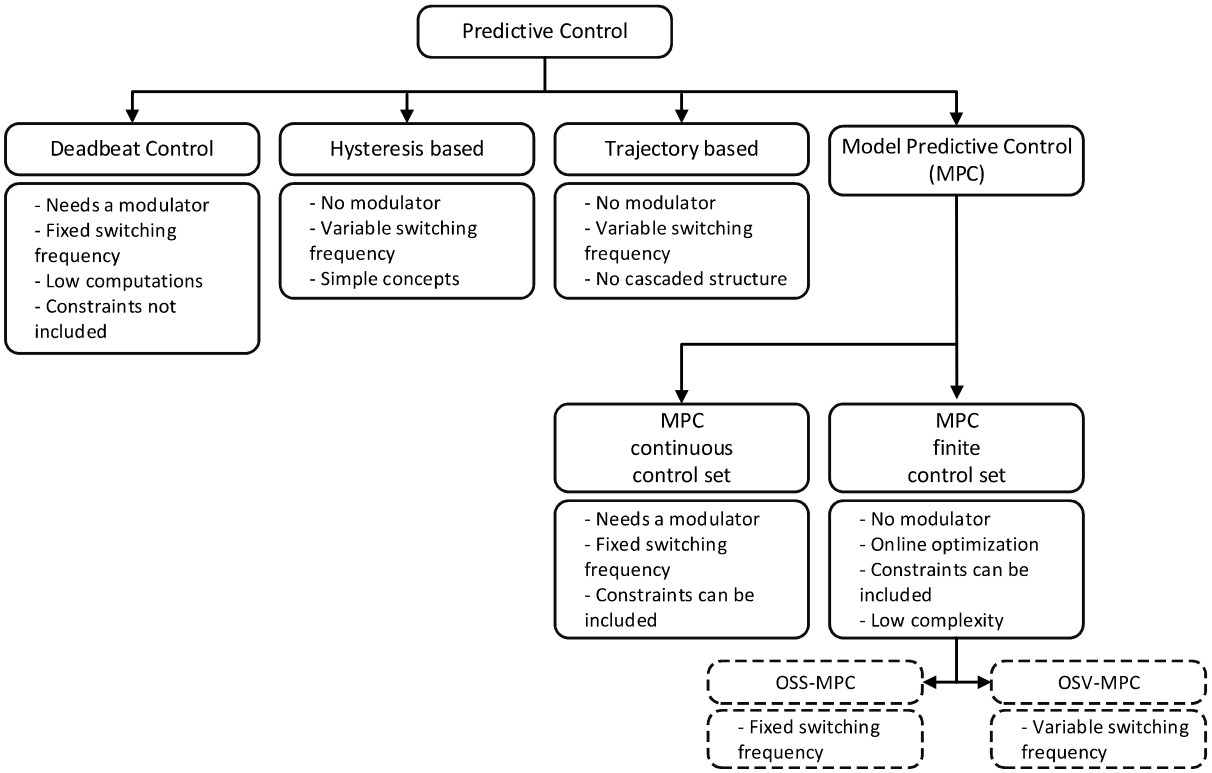


Figure 4-1– Classification of predictive control methods used in power electronics [70, 63].

It is important to note that the deadbeat control and the MPC with continuous control set require a modulator to generate the necessary signal, thus producing a fixed switching

frequency, while the other controllers directly produce the signals for the semiconductor switches, not requiring modulators, producing a variable switching frequency [63], but there are some techniques to correct this characteristic [75].

In addition to the simplicity and intuitiveness of implementing predictive control, some non-linearities of the system can also be included in the model, avoiding the need to linearize the model for a given point of operation and improve the system's operation for all conditions. Besides, there is the possibility of including restrictions on some variables when designing the controller, as well as some penalty criteria [63].

In addition to the no need for a high-frequency modulator, the listed implementation simplicity assisted the choice of Model Predictive Control – Finite Control Set, as a predictive control technique used in this thesis.

4.2 MPC Basic Principles

Among the control techniques more advanced than the classic PID control, MPC is the most successful industrial application. Although the concept of MPC refers to the 1960s as an application of the optimal control theory, the use in the chemical industry only started in the late 1970s, since the time intervals involved in the processes were sufficiently large to perform the necessary calculations [63, 69, 76, 77, 78].

The use of MPC in power electronics started in the 1980s in applications that lacked low switching frequency since higher switching frequencies require many calculations and, consequently, computational effort, unavailable at the time. Thus, with the development of increasingly faster microprocessors capable of carrying out large numbers of mathematical operations, interest in the use of MPC in applications with the high switching frequency previously unviable has intensified [63, 71].

The MPC does not represent a specific control strategy. It encompasses a concept that describes various controllers that feature the use of a system model to predict the future behavior of variables up to a predetermined time horizon and their selections to provide a cost function with minimum value [63, 69].

This structure has several advantages, such as:

- The wide variety of systems to which it can be applied;
- the use of intuitive and straightforward concepts;
- the possibility of using multivariable cases;

- the possibility of compensating for deadtime;
- the ease of including non-linearities in the model;
- the simple treatment of possible restrictions and penalties;
- the easy implementation, easy customization, among others [63].

However, some crucial disadvantages must be taken into account, such as:

- the significant computational effort required, with large amounts of mathematical calculations when compared to classic controllers;
- the direct influence of the model's fidelity on the result, and the fact that changes in the model's parameters during execution may lead to difficulties in adapting the algorithm [63].

As previously mentioned, the predictive control methods are divided into two classes regarding the nature of the optimization problem [67], as shown in Figure 4-2.

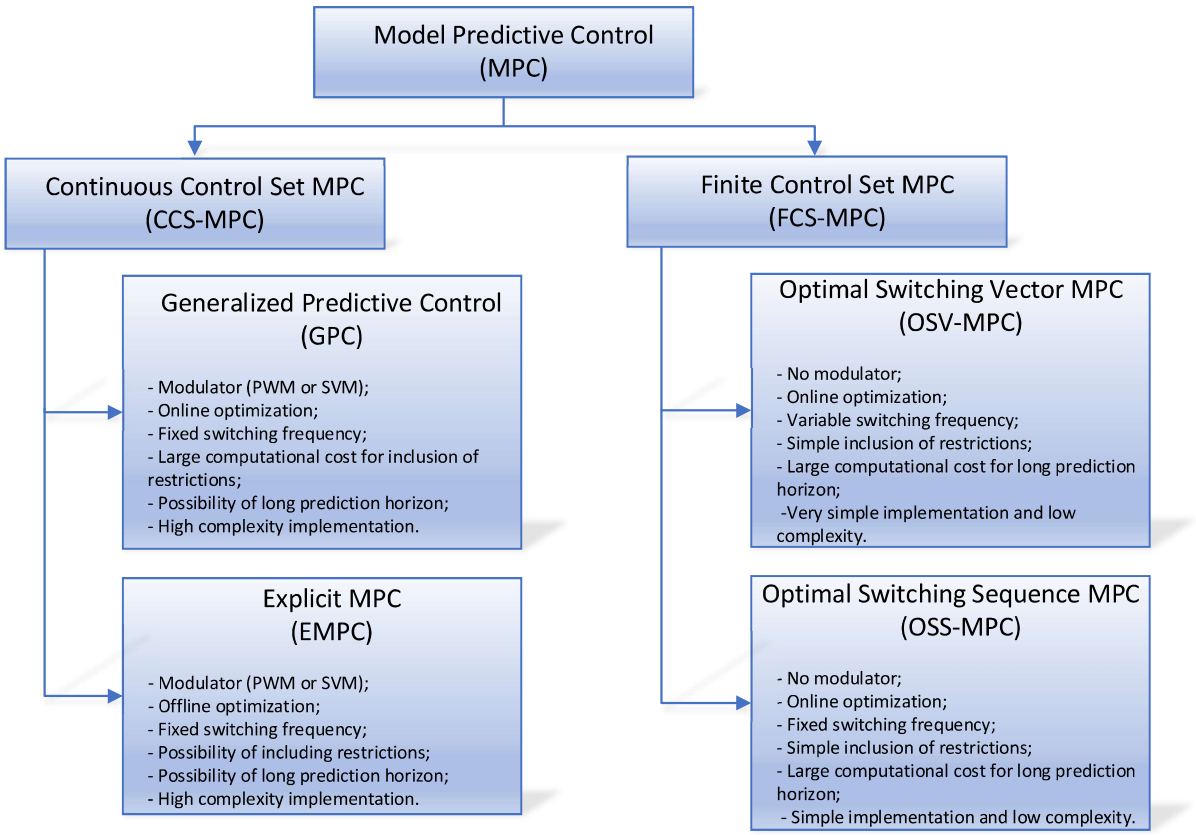


Figure 4-2– Classification of MPC methods [63, 79].

The class named Continuous Control Set MPC (CCS-MPC) generates a continuous control signal over time. Then a modulation technique is used to produce the switching pulses of the converter [67]. The most used predictive control strategies in this class are Generalized Predictive Control (GPC) and Explicit MPC (EMPC), and the great advantage of these techniques is the operation with a fixed switching frequency. However, their implementation complexity is high [67].

The second class of predictive control, known as the Finite Control Set MPC (FCS-MPC), takes into account the discreet characteristics of the power electronics performance converters making their implementation much simpler for this type of application. Also, this class does not require modulation techniques to act on the converter [67, 79]. In the literature, two types of controllers belonging to the FCS-MPC class are found: Optimal Switching Vector MPC (OSV-MPC) and Optimal Switching Sequence MPC (OSS-MPC).

The OSV-MPC, the first predictive control strategy adopted in power electronics applications, is still the most widely used today [71] due to its low implementation complexity and rapid dynamic response [67]. However, it presents as a disadvantage the fact that it presents a variable switching frequency. However, some studies aim to minimize the dispersion of the frequency harmonic spectrum through the cost function [62, 79].

OSS-MPC considers a control set composed of a limited number of possible switching sequences per switching period. In this way, OSS-MPC takes the time into account as an additional decision variable. Thus, the instant the switches change state, they compose an output signal with fixed switching frequency [67].

4.2.1 MPC for Power Electronics

Due to the advancement in the development of increasingly fast and powerful microcontrollers and microprocessors, the MPC theory, developed over fifty years ago, has become widely used in power electronics applications, which require short sampling times and a significant number of mathematical operations to be developed [67, 63].

Power electronics-based systems have as their main characteristic the finite number of switching states, so in power electronics converters, the control action is limited to the set of switching states possible in the converter, making the MPC an option feasible and easy to implement. Its cost function is directly associated with the set of variables controlled [63, 79].

At each sampling time, the fast microprocessors of the digital controller perform various calculations and predict the future of the variables for each possible switching state based on

the predictive model, measurements, and system states. Then, the switching state with the lowest cost is applied to the converter. Thus, this control technique is intrinsically linked to the switching process, dispensing the use of a modulation technique [63, 79].

Although the MPC is an open-loop optimization algorithm, when repeated at each sampling time, it behaves like a feedback loop control based on optimization, making its dynamic response quick in the face of reference variations or disturbances [63, 79].

About SDC-CHB, due to its low implementation complexity, the non-need to use modulation techniques for firing the semiconductor switches, and the several undesirable short- circuits switching states, the OSV-MPC makes an attractive control strategy for this type of application, being chosen to verify the technical feasibility of controlling the topology proposed by this work.

The basic OSV-MPC diagram is shown in Figure 4-3, where x^k are the important measure to the system at the time instant k; $x^{p(k+1)}$ are the predictions built by the predictive model for each of the N converter switching states combination at the time instant $k+1$, while p is the index of this prediction; $x^*$are the reference signal to be compared; and $S_{opt}(t_k)$ is the optimal switching state applied to the converter [63].

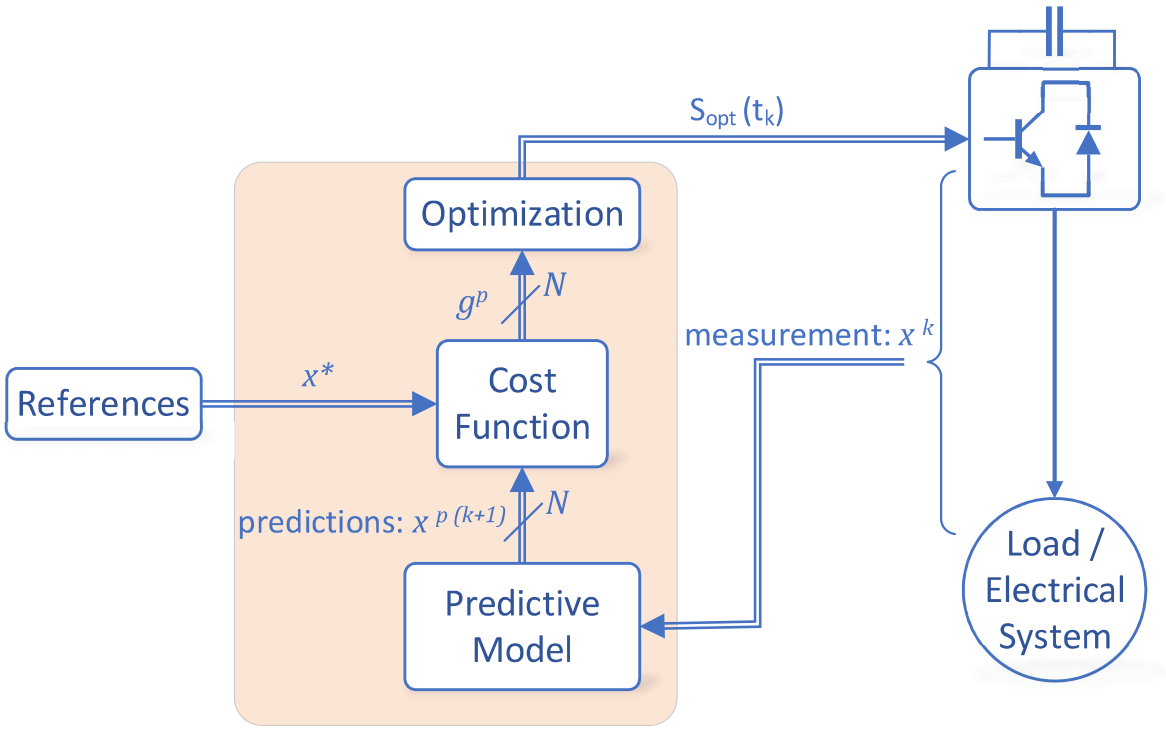


Figure 4-3– Basic OSV-MPC scheme [63].

The sequential algorithm of Figure 4-3 is presented in Figure 4-4 in the form of a flowchart, where, in the time arrow, the past, present, and future time instants are represented by $k-1, k$ and $k+1$, respectively. The following actions are performed on the time step of duration k [79]:

- the readings of the variables represented as x^k, are performed;
- references x^* are calculated;
- a loop scan is performed (which consumes most of the computational effort of the algorithm):
  - x^p is the set of predicted variables x^{k+1} calculated for each N switching states;
  - the cost function g^p is calculated for each x^p calculated;
- optimization with choice of the minimum value of the cost function g^{min};
- application in the converter of the optimal switching vector for $k+1$ time instant.

This strategy guarantees an optimized response and is much faster the greater the microcontroller's capacity to process it for shorter and shorter time steps [79].

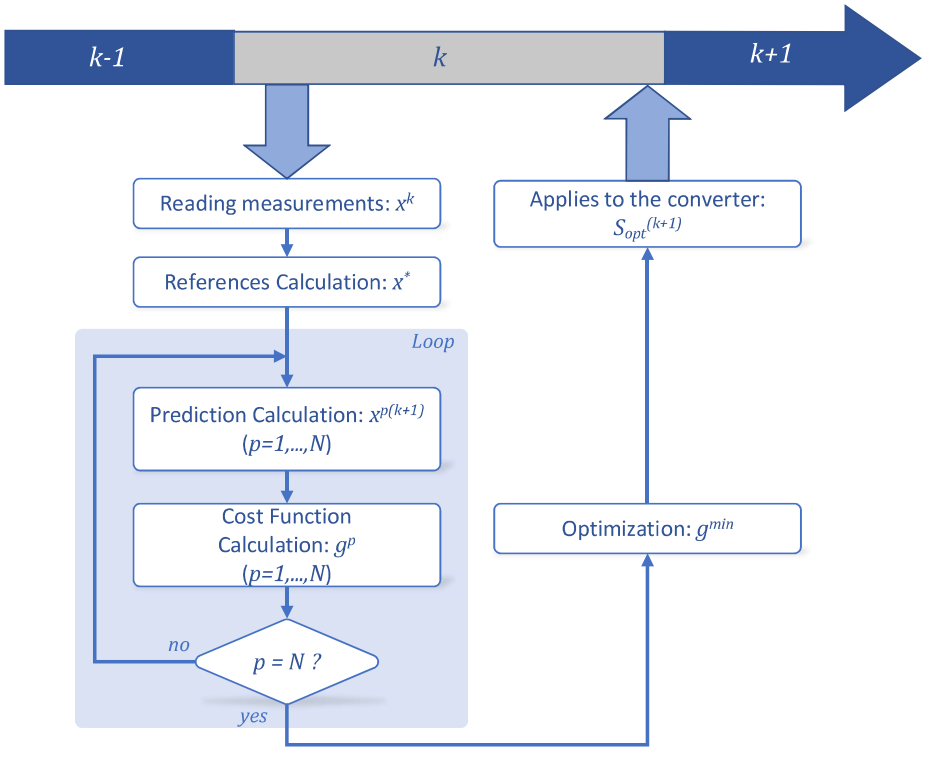


Figure 4-4– Basic OSV-MPC flowchart [63, 79].

As previously mentioned, OSV-MPC has several advantages for power electronics applications, such as fast dynamic response and the ease of adding restrictions, penalties, and non-linearities, increasing its flexibility and facilitating its implementation. However, due to the high sampling frequency required for implementing this control technique, high computational capacity is required compared to classical linear control techniques [80, 81, 82].

The OSV-MPC operation also features an operation with variable switching frequency due to how the cost function is calculated, making the design of filters more difficult, increasing the probability of problems related to resonance [79, 67, 83, 84, 85].

Besides, for this type of predictive control technique, the model reliability to be controlled is critical and may present erroneous predictions if incorrect parameters are used, thus impairing the final result, often making it unfeasible [67, 83, 84, 86]. Thus, by presenting well-known and studied plant models, the MPC is mainly used for power electronics applications, presenting robust results [87, 88, 89].

4.3 SDC-CHB STATCOM

4.3.1 STATCOM

STATCOM is an advanced power electronics equipment that is used for reactive power compensation. Its function is to provide voltage support in critical areas of the power system. The predecessor of the static synchronous compensator, that is, the rotary synchronous compensator, has been widely used in the past for reactive shunt compensation. The rotary compensator has several desirable functional characteristics, such as injecting high capacitive currents during undervoltage transient periods and having an inductive internal impedance, whose typical values do not cause resonance with the transmission grid. However, the rotary compensator has some disadvantages, such as slow response time, rotational instability, low short circuit impedance, and frequent maintenance. Furthermore, it does not meet the modern requirements for flexibility in real-time control of power flow, within the new concepts of FACTS systems, like flexible control, faster response, reduced stress, and losses in the system [90, 91].

STATCOM is the electronic equivalent of the ideal synchronous compensator and is a shunt-connected device that generates capacitive or inductive current independent of the system voltage, is also used for control of PCC (point of common coupling) voltage [90, 92, 93].

Figure 4-5 consists of a simplified diagram of the STATCOM connection in a grid, showing the PCC and its voltage U_{PCC}, the connection reactance X_{ST}, the STATCOM voltage U_{ST}, its drained current I_{ST}, and the voltage drop ΔU_x produced in theX_{ST} reactance.

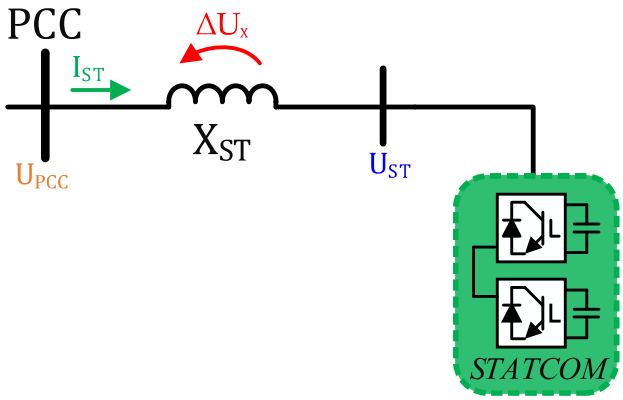


Figure 4-5– Simplified STATCOM diagram [94]

The active and reactive power equations referring to Figure 4-5 are shown by (5) and (6), where δ is the phase shift angle between U_{PCC} and U_{ST}voltages [95, 96].

$$P_{PCC} = \frac{U_{PCC} \cdot U_{ST}}{X_{ST}} \cdot \sin\delta \qquad (5)$$

$$Q_{PCC} = \frac{U_{PCC}^2 - U_{PCC} \cdot U_{ST}}{X_{ST}} \cdot \cos\delta \qquad (6)$$

Considering (5) and (6) there are five relevant situations [94], and the STATCOM operation can be based on more than one of them simultaneously:

a) U_{ST} voltage leads the U_{PCC} voltage, this is, $0° < \delta < 90°$: active power flows to PCC;

b) U_{PCC} voltage leads the U_{ST} voltage, this is, $-90° < \delta < 0°$: active power flows to STATCOM;

c) U_{PCC} voltage has the same phase as U_{ST} voltage, this is, $\delta = 0°$, and $|U_{PCC}| > |U_{ST}|$: there is no active power flowing, but the reactive power flows to STATCOM (inductive mode);

d) U_{ST} voltage has the same phase as U_{PCC} voltage, this is, $\delta = 0°$, and $|U_{PCC}| < |U_{ST}|$: there is no active power flowing, but the reactive power flows to PCC (capacitive mode);

e) U_{ST} voltage has the same phase as U_{PCC} voltage, this is, $\delta = 0°$, and $|U_{PCC}| = |U_{ST}|$: there are no active or reactive power flowing (idle mode);

As this thesis proposes the STATCOM operation only in inductive and capacitive modes, that is, without active power flow control, except for the capacitors DC-link and the device conductivity losses, the situations (a) and (b) will not be addressed, producing characteristic curves similar to those observed in Figure 4-6 and Figure 4-7. The curves cross the vertical axis the moment $U_{ST} = U_{PCC}$, being parameterized by this last index.

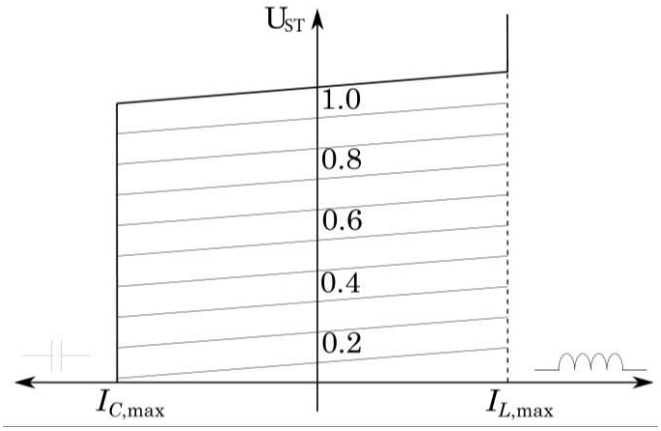


Figure 4-6– STATCOM U − I Characteristics [97, 98, 99]

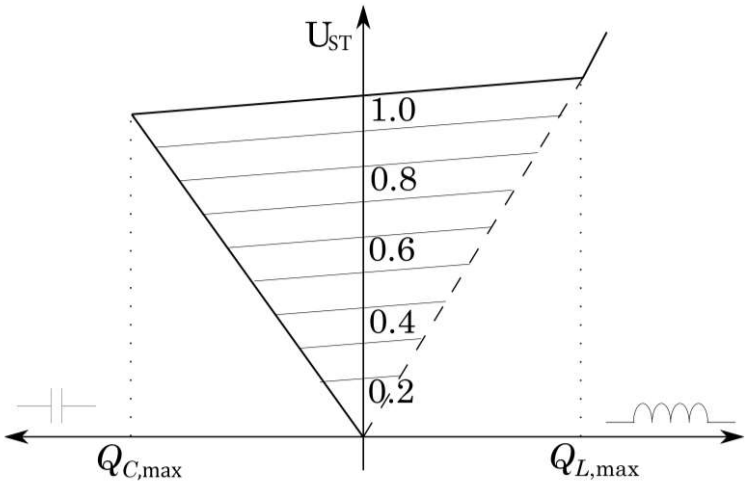


Figure 4-7– STATCOM U − Q Characteristics [97, 100]

According to (5) and (6), Figure 4-6 illustrates situations (c) and (d) mentioned above, where the STATCOM can perform inductive or capacitive compensation regarding its line current, this is, when $|U_{PCC}| < |U_{ST}|$, STATCOM generates reactive power, while when $|U_{PCC}| > |U_{ST}|$, the equipment absorbs reactive power [94]. These presents that the STATCOM can be operated over its full output current range even at very low system voltage levels. This is, the maximum capacitive or inductive STATCOM output current can be maintained independently of the AC system voltage, and the maximum reactive generation or absorption changes linearly with the AC system voltage [100].

Similarly, Figure 4-7 presents the U-Q characteristic, which shows that STATCOM can provide capacitive or inductive power even at very low voltages [96].

4.3.2 STATCOM Model Predictive Control

Figure 4-8 presents the overview operation of the OSV-MPC applied to the SDC-CHB with a STATCOM application, which e_{Sn} and i_{Sn} are the measured voltages and currents source, U_{DCn} are the measured DC-link voltages, U_{DCn}^{*} are the DC-link voltage references, U_n are the synthetized STATCOM voltages, $P(k+2)$ and $Q(k+2)$ are the predicted active and reactive powers, $p_{loss}(k+2)$ is the required change in the active power flow to regulate the DC-link capacitor voltage [101, 102, 7], $P^{*}(k+2)$ and $Q^{*}(k+2)$ are the active and reactive reference powers, k and $k+2$ is the actual and predicted states after two time steps to compensate the processing delay signals, N is the total prediction states, S_{opt} is the optimal switching state and n is the phase to which it refers (a, b or c).

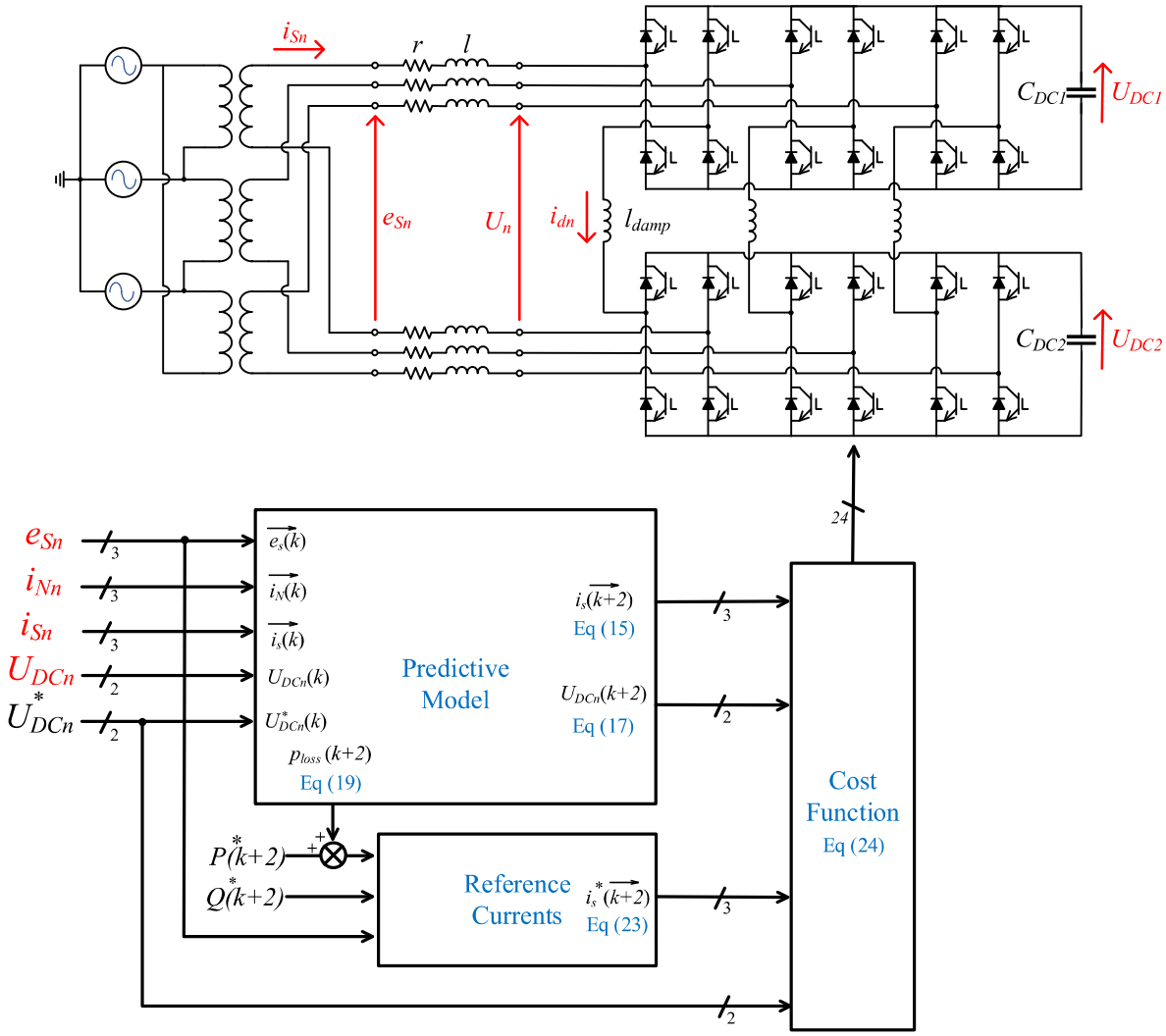


Figure 4-8– Graphical description of SDC-CHB STATCOM topology using MPC [7].

The STATCOM basic mathematical development using SDC-CHB topology is demonstrated as follows, in which C_{DCk} is the DC-link capacitor voltage, r and l are the RL resistance and inductance filter, l_{damp} is the damping inductors to reduce the current peak between upper and lower H bridge modules, using empirically obtained values [11, 103, 7]; and, i_{dn} are the currents measured in these inductors.

Thus, the STATCOM voltage U_n, considering C_{DC1} and C_{DC2} with the same voltage value (U_{DC}), can take on $[-2U_{DC,} - U_{DC}, 0, +U_{DC}, +2U_{DC}]$ values, that is, five voltage levels. However, it is essential to point out that the MPC uses the present and predicted DC-link voltage values to perform the calculations [104, 105, 7].

4.3.3 Current loop prediction

Based on Figure 4-8, the current equation in the RL filter loop is given by (7) using the Kirchhoff voltage law [11, 101, 7]:

$$e_{Sn} - 2l\frac{di_{Sn}}{dt} - 2ri_{Sn} - U_n = 0 \quad (7)$$

Applying regressive Euler's numerical integration method, the discrete system equation is presented on (8), being T_s the sample time for discretizing.

$$e_{Sn}(k) - \frac{2l}{T_s}\left(i_{Sn}(k) - i_{Sn}(k-1)\right) - 2ri_{Sn}(k) - U_n^N = 0 \quad (8)$$

For the continuation of the mathematical development, it must be considered that the source voltage value is the same for the next time step. These estimates are due to the power grid frequency being much lower than the switching frequency [22, 102, 7].

With these approaches, the model can be simplified, and, after mathematical development, equations (9) to (11) are obtained. Equation (11) represents the predicted current.

$$e_{Sn}(k) - \frac{2l}{T_s}\left(i_{Sn}(k+1) - i_{Sn}(k)\right) - 2ri_{Sn}(k) - U_n^N(k+1) = 0 \quad (9)$$

$$\left(\frac{2l}{Ts}\right)i_{Sn}(k+1) = e_{Sn}(k) + \frac{2l}{T_s}i_{Sn}(k) - 2ri_{Sn}(k) - U_n^N(k) = 0 \quad (10)$$

$$i_{Sn}(k+1) = \frac{T_s}{2l}\left(e_{Sn} + \frac{2l}{T_s}i_{Sn}(k) - 2ri_{Sn}(k) - U_n^N(k)\right) \quad (11)$$

The term U_n^N represents the STATCOM module voltage multiplied by the respective switching function $S_{nx}(k)$, which x is the module index (upper or lower) according to equation (12):

$$U_n^N(k) = S_{n1}(k) \cdot U_{DC1}(k) + S_{n2}(k) \cdot U_{DC2}(k) \quad (12)$$

The function $S_{nx}(k)$ represents all possible switching states in each converter module, equal to $-1, 0,$ or 1 respectively, when a negative, neutral or positive voltage is produced at the module output.

As the voltage drop over the damping inductors l_{damp} are small and have little influence on the U_n^N voltages result, this term was disregarded in the equation (12). However, the electric current flowing through this inductor will be considered when determining the DC-link capacitor voltage.

4.3.4 DC-link voltage prediction

The predicted DC-link capacitor voltages, $U_{DCx}(k+1)$, can be obtained taking into account its present value as well the current contribution of each phase [102, 104], relating them to the capacitance value and its switching functions, presented on (13), where C is the DC-link capacitance. The function $S_{ndx}(k)$ represents the switching state related to the switches that are connected to the damping inductors l_{damp}. Since the capacitor voltages are also obtained by the currents flowing between them, the $i_{dn}(k)$ currents have to be considered, as well as the state of their switches.

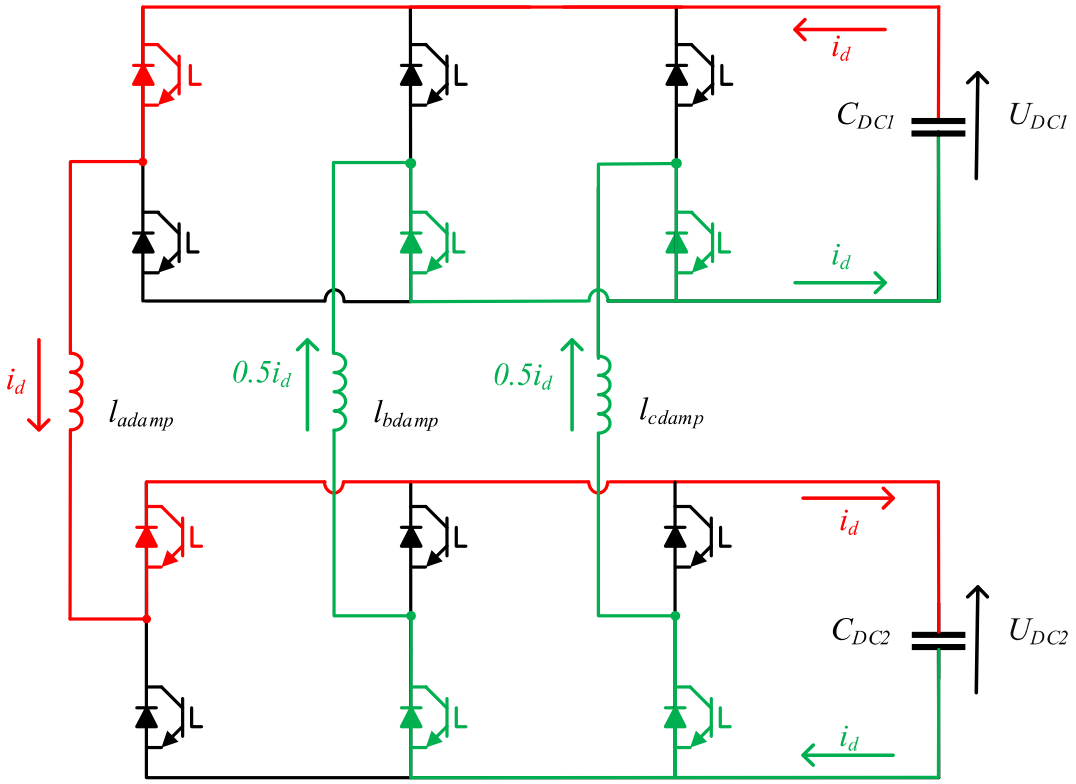
$$U_{DCx}(k+1) = U_{DCx}(k) + \frac{T_s}{C}\left(S_{ax} \cdot i_{Sa}(k) + S_{bx} \cdot i_{Sb}(k) + S_{cx} \cdot i_{Sc}(k)\right) - \\ - \frac{T_s}{C}\left(S_{adx} \cdot i_{da}(k) + S_{bdx} \cdot i_{db}(k) + S_{cdx} \cdot i_{dc}(k)\right) \quad (13)$$

4.3.5 Damping inductor current prediction

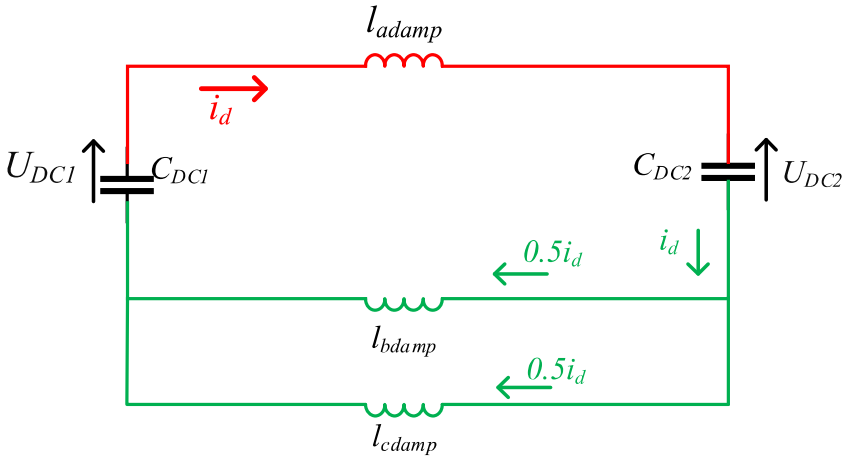
The current flowing through the damping inductors l_{damp} is based on the potential difference between the two STATCOM capacitors and the combination of semiconductor switches that interconnect these components. Thus, it is essential to note that the states of the switches must provide a round trip path for current flow to occur between the capacitors. After analyzing all possible and allowed switching states, it was observed that the electric currents flowed through the three l_{damp} or flow through none, thus excluding the possibility of only one leg with inductance being disconnected.

In this way, it can be inferred that the electric current in one direction will be concentred on only one inductor. In contrast, in the opposite direction, it will be divided between two

inductors. Figure 4-9 (a) illustrates this condition, where, for example, a current of magnitude I_d flows between capacitors C_{DC1} and C_{DC2}. On the l_{adamp} inductor it maintains its module, however, it is divided equally between the l_{bdamp} and l_{cdamp} inductors. Figure 4-9 (b) shows the equivalent circuit of this condition.



(a)



(b)

Figure 4-9– Current path between capacitors.

Thus, considering that $l_{adamp} = l_{bdamp} = l_{cdamp} = l_{damp}$, it can be observed that the equivalent series inductance of the path formed by where the I_d current flows is $1.5 \cdot l_{damp}$.

Based on Figure 4-9 (b), the current equation in the RL filter loop is given by (14) using the Kirchhoff voltage law, where S_{dx} represents the possible switching states which determine the current direction:

$$S_{Nx}\,(U_{DC1} - U_{DC2}) - 1.5 l_{damp} \frac{di_{Nn}}{dt} = 0 \qquad (14)$$

Applying Euler's numerical integration method, the discrete system equation is presented on (15), being T_s the sample time for discretizing.

$$S_{Nx}\left(U_{DC1}(k) - U_{DC2}(k)\right) - \frac{1.5 l_{damp}}{T_s}\left(i_{dn}(k) - i_{dn}(k-1)\right) = 0 \qquad (15)$$

Continuing the mathematical development, equation (16) is obtained, representing each leg l_{damp} current:

$$i_{Nn}(k+1) = \frac{T_s}{1.5 l_{damp}} \cdot S_{dx}\left(U_{DC1}(k) - U_{DC2}(k)\right) + i_{Nn}(k) \qquad (16)$$

4.3.6 Variable prediction for $(k+2)$

At the k^{th} time instant, the MPC performs a scan through equations (11) and (13) and uses the converter inherent switching function $S_{nx}(k)$, to predict the currents determined by $i_{Sn}(k+1)$ and the converter voltages expressed by $U_{DCx}(k+1)$. Afterward, a cost function is computed, using a combination between the reference signals and the predicted values, thus, selecting the optimal control by choosing the switching states that produce the lowest cost function value.

However, this strategy implementation in practice can only be applied in the $(k+1)^{th}$ time instant due to the hardware computational delay [106, 102]. Thus, a step time delay must be inserted in the system to compensate for this peculiarity.

Therefore, at the k^{th} time instant, the MPC computes the $(k+1)^{th}$ system state through the equations (11) and (13). Subsequently, the control effects a new scan but this time using the calculated $(k+1)^{th}$ values to predict the $(k+2)^{th}$ values, represented through (17) to (19), only then the cost function is calculated, and the optimal vector is chosen [102, 107].

$$i_{Sn}(k+2) = \frac{T_s}{2l}\left(e_{Sn} + \frac{2l}{T_s} i_{Sn}(k+1) - 2r i_{Sn}(k+1) - U_n^N(k+1)\right) \quad (17)$$

$$U_n^N(k+1) = S_{n1}(k+1) \cdot U_{DC1}(k+1) + S_{n2}(k+1) \cdot U_{DC2}(k+1) \quad (18)$$

$$\begin{aligned} U_{DCx}(k+2) &= U_{DCx}(k+1) + \\ &+ \frac{T_s}{C}\left(S_{ax} \cdot i_{Sa}(k+1) + S_{bx} \cdot i_{Sb}(k+1) + S_{cx} \cdot i_{Sc}(k+1)\right) - \\ &- \frac{T_s}{C}\left(S_{adx} \cdot i_{da}(k+1) + S_{bdx} \cdot i_{db}(k+1) + S_{cdx} \cdot i_{dc}(k+1)\right) \end{aligned} \quad (19)$$

4.3.7 References generation and power calculation

When the reference signals are calculated, the coupling between the active power and the voltages of the DC-link capacitors must be taken into account. That is, the DC-links regulation requires an extra active power amount that causes an additional active power flow related to the capacitors to keep these voltages close to the set reference values [11, 102]. This real power p_{loss} is the sum of each capacitor power portions p_{DCx}, shown in equations (20) and (21) [102].

$$p_{DCx}(k+2) = \frac{C}{T_s}\left[\left(U_{DCx}{}^*(k+2)\right)^2 - \left(U_{DCx}(k+1)\right)^2\right] \quad (20)$$

$$p_{loss}(k+2) = \sum_{x=1}^{2} p_{DCx}(k+2) \quad (21)$$

The system operator determines the active and reactive reference powers, $P^*(\mathrm{k}+2)$ and $Q^*(\mathrm{k}+2)$, and uses to reference currents calculation through instantaneous power theory

[108]. The required capacitor power p_{loss} is added to active power reference becoming in the total active power reference $P^*_{T(K+2)}$, as shown in equation (22).

$$P^*_T(k+2) = p_{loss}(k+2) + P^*(k+2) \quad (22)$$

In the STATCOM developed in this work, the active reference power $P^*(k+2)$ was null, being used only that enough to supply the internal capacitors losses (16). An author's free choice pattern provides the reactive power reference to cover situations of reactive supply and consumption, however $Q^*(\mathrm{k}+2)$ can be originated according to the end-user needs, either through a power factor control or any other desired.

Thus, $P^*_T(\mathrm{k}+2)$, $Q^*(\mathrm{k}+2)$, and e_{Sn} pass through a $\alpha\beta$-current transformation and then through an inverse Clarke transformation to build the reference currents $i^*_{sn}(k+2)$ [108], as are expressed from (23) to (25).

$$\begin{bmatrix} e_{S\alpha}(k+1) \\ e_{S\beta}(k+1) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} e_{Sa}(k+1) \\ e_{Sb}(k+1) \\ e_{Sc}(k+1) \end{bmatrix} \quad (23)$$

$$\begin{bmatrix} i^*_{S\alpha}(k+2) \\ i^*_{S\beta}(k+2) \end{bmatrix} = \Delta \cdot \begin{bmatrix} e_{S\alpha}(k+1) & e_{S\beta}(k+1) \\ e_{S\beta}(k+1) & -e_{S\alpha}(k+1) \end{bmatrix} \begin{bmatrix} P^*_T(k+2) \\ Q^*_T(k+2) \end{bmatrix} \quad (24)$$

Where:

$$\Delta = \frac{1}{e_{S\alpha}(k+1)^2 + e_{S\beta}(k+1)^2}$$

$$\begin{bmatrix} i^*_{Sa}(k+2) \\ i^*_{Sb}(k+2) \\ i^*_{Sc}(k+2) \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i^*_{S\alpha}(k+2) \\ i^*_{S\beta}(k+2) \end{bmatrix} \quad (25)$$

4.3.8 Cost Function

The MPC cost function's main objective applied to STATCOM is to scan all possible switching combinations and choose which state has the smallest error between the reference currents and the predicted currents and the slightest error between the reference and the predicted DC-link capacitor voltages. However, since prohibitive states are to be avoided, there may also be a penalty in the cost function, being excluded in this work.

The expression for the cost function adopted in this study is shown on (26), where g^N is the cost for all the switching state, W_{ia}, W_{ib}, W_{ic}, W_{UDC1} and W_{UDC2} are the weight factors and P_{en} is the described penalty [102].

$$\begin{aligned} g^N = {} & W_{ia}[i_{sa}^*(k+2) - i_{sa}(k+2)]^2 + W_{ib}[i_{sb}^*(k+2) - i_{sb}(k+2)]^2 + \\ & + W_{ic}[i_{sc}^*(k+2) - i_{sc}(k+2)]^2 + W_{UDC1}[U_{DC1}^*(k+2) - U_{DC1}(k+2)]^2 \\ & + W_{UDC2}[U_{DC2}^*(k+2) - U_{DC2}(k+2)]^2 + P_{en} \end{aligned} \quad (26)$$

In this thesis, a null active power reference, $P^*(\mathrm{k}+2) = 0$, was used to obtain the equipment behavior only as a provider of reactive power as STATCOM. Furthermore, as all possible converter states are known, whether they are prohibitive or not, it was decided to use only the switching states that do not cause short circuits in equipment, saving computational processing and thus suppressing the term P_{en} in equation (26) [11].

Chapter 5: Experimental Results

To demonstrate not only the SDC-CHB superiority over the classic CHB but also its technical feasibility, experimental results of both structures were compared on a real-time platform. The topologies were applied as a STATCOM device with similar characteristics and the same voltage and current levels for the experiment.

Both converters are configured with five levels of phase voltage, connected in a $400V\ rms$ grid voltage, and providing $\pm 25kvar$ reactive power. The OSV-MPC controls the SDC-CHB described previous, and the CHB uses a classical set of linear controls, with a combination of global and cluster DC voltage balancing, well established in the literature [9, 109], combined with a classical multicarrier phase shift pulse width modulation (PSPWM) [34, 110].

5.1 Real-time Platform

A powerful Hardware-In-the-Loop (HIL) platform has been used to experimentally investigate the SDC-CHB STATCOM operation [111, 112]. The OPAL-RT 5700, using a potent processor, can allow a high-frequency drive solution that provided complete OSV-MPC implementation and the complete power plant emulation through the eFPGASIM tool present in the equipment.

This HIL implementation has an optional computer as supervisor, connected to the hardware, setting the references and some element values, with access to the generated waveforms. The signals were obtained through the signal acquisition boards and the oscilloscope Yokogawa DL750 connected to I/O ports. This architecture is shown in Figure 5-1 (a), and the implementation image in Figure 5-1 (b).

As previously mentioned, the computational hardware delay considered is one time step, being necessary to perform all calculations and comparisons related to $(k+1)^{th}$ values and to predict the $(k+2)^{th}$ states system [111, 112].

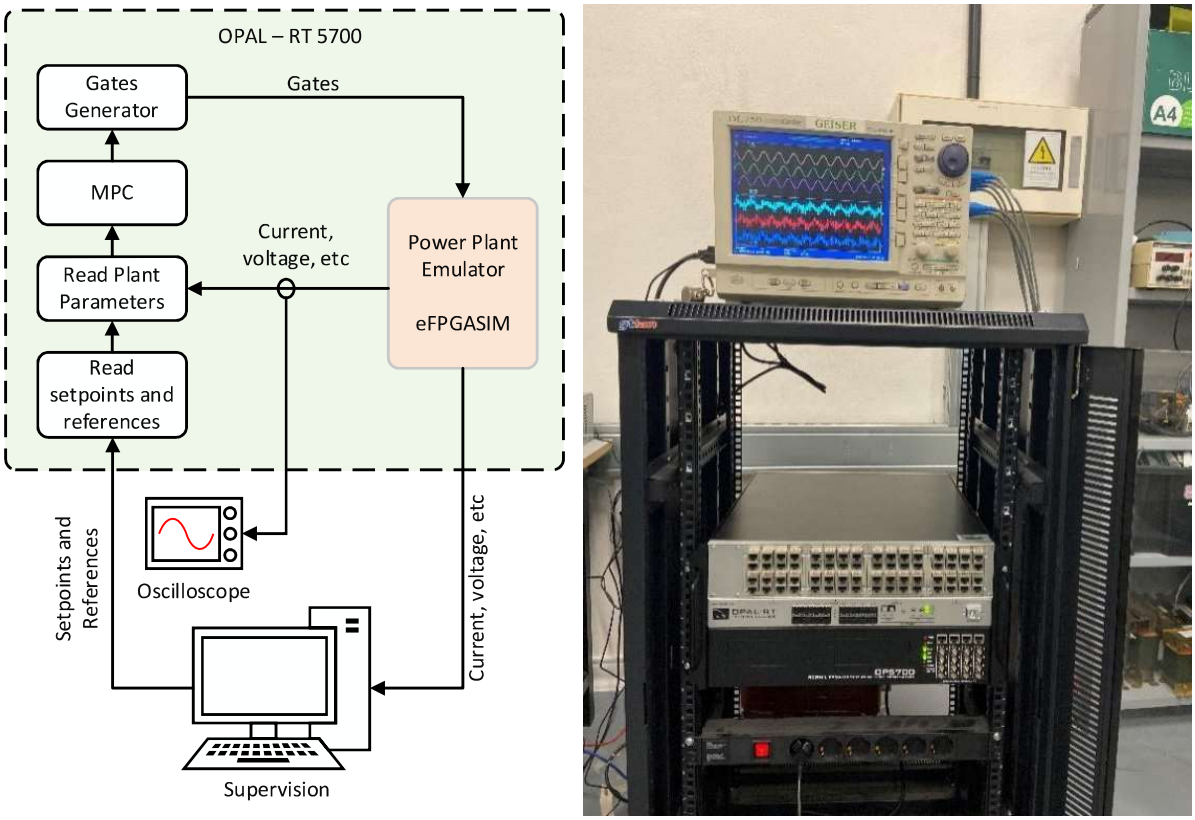
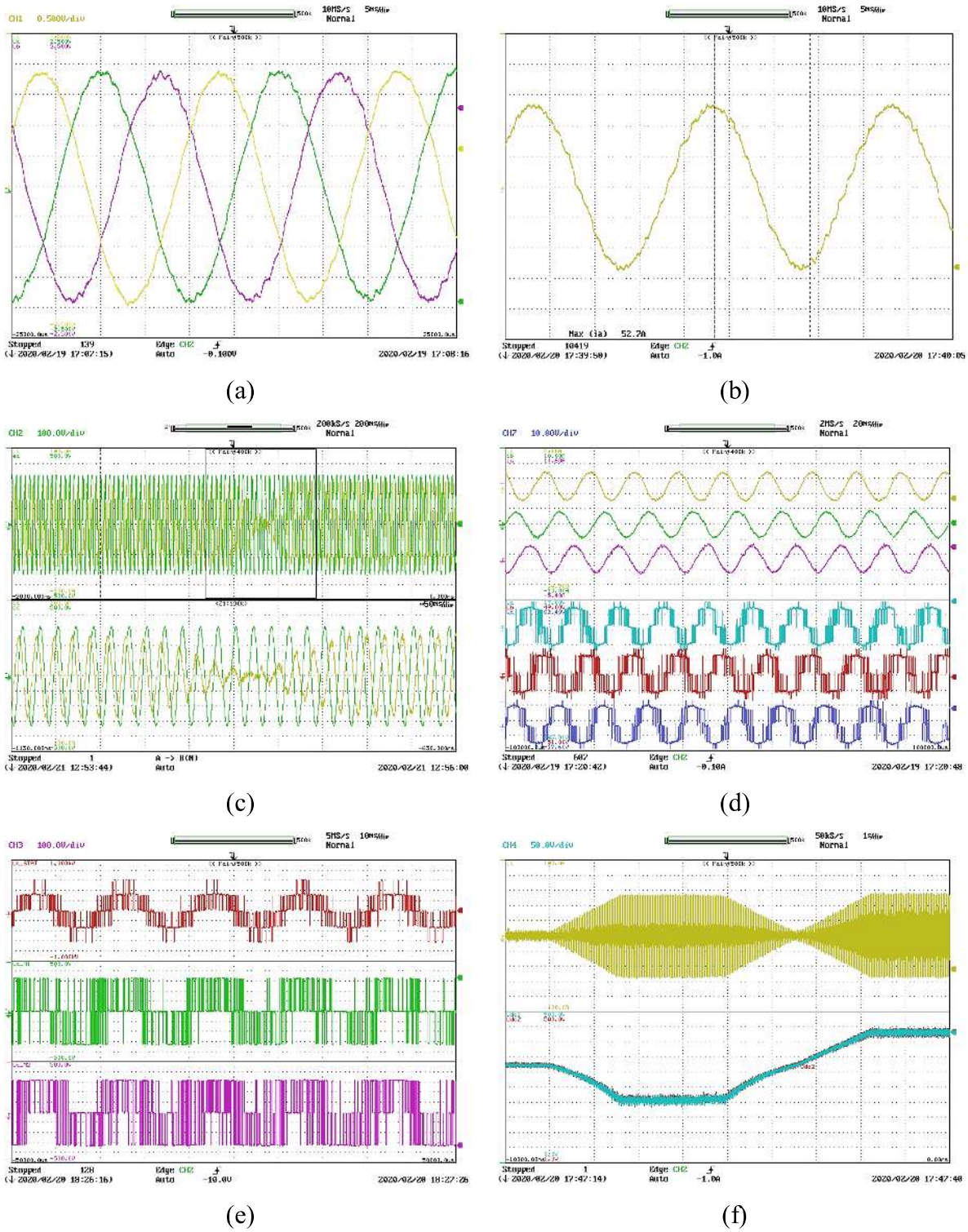


Figure 5-1– Hardware-In-the-Loop implementation: (a) OPAL-RT 5700 Flowchart; (b) Implementation image with emphasis on signals in the oscilloscope [7].

Some experimental results were obtained on the OPAL-RT 5700 platform through signal acquisition boards. The Yokogawa DL750 oscilloscope screens are shown in Figure 5-2, where it is possible to observe the synthesis of the grid current and the STATCOM voltage signals, and the voltage variation of the DC-link of the capacitors.



(a) (b)

(c) (d)

(e) (f)

Figure 5-2– Experimental results: (a) three-phase grid currents; (b) one phase grid current; (c) one phase grid current in changing mode; (d) grid currents and synthesized STATCOM voltages in the same screen; (e) synthesized STATCOM voltage and its voltage per module; (f) capacitor DC-link voltages variation [7].

5.2 The system implementation

The five-level SDC-CHB and the CHB experimental results configured as STATCOM are verified through implementation in OPAL-RT 5700 to demonstrate the proposal viability.

Thus, two comparisons between the converters were developed: one with equal DC-link voltage ripple values; and the other with equal individual capacitance values.

When using a $1 \cdot 10^{-4} s$ time step (T_s) to call the OSV-MPC functions, the control analyzes the need or not to change the state of any switch, thus producing a variable switching frequency that is not expressed precisely by the T_s value. As the SDC-CHB OSV-MPC provides the semiconductor switches activation in the three phases simultaneously, it was necessary to observe the average number of changes per cycle per phase produced by the converter with the adopted time step value. Thus, for a CHB PSPWM, a $2\ kHz$ carrier frequency was chosen to generate the same 40 switchings per cycle per phase observed in the SDC-CHB OSV-MPC with $1 \cdot 10^{-4} s$ T_s. It is important to point out that this value depends on the inductances at the converter terminals, and may change if any inductor is changed.

5.2.1 Equal DC-link voltage ripple

This comparison between CHB and the proposed topology uses the same DC-link voltage ripple per capacitor to observe the difference in design capacitance values.

The following equation (1) was used to design the CHB capacitors, where the maximum ripple is designed for $11V$; the DC-link voltage average is $300V$; the angular frequency is $2 \cdot \pi \cdot 50$; and the power is $25kW$.

According to (1):

$$C_{CHB} = \frac{25 \cdot 10^3}{2 \cdot \pi \cdot 50 \cdot 300 \cdot 11} = 24{,}114.4\mu F \approx 24{,}000\mu F \qquad (27)$$

This is, since the CHB has 6 capacitors, each device has approximately $4{,}000\mu F$. Thus, for this experiment, all ripple values (in CHB and SDC-CHB topology) are equal, approximately 11V.

5.2.2 Equal Capacitance

This comparison between CHB and the SDC-CHB topologies uses the same capacitance values per capacitor to observe the difference in the DC-link voltage ripple.

Equation (2) was used to dimension the proposed topology capacitors, where the maximum ripple designed is $11V$; the other parameters are the same as the previous implementation.

According to (2):

$$C_{SDC-CHB} = \frac{25 \cdot 10^3}{10 \cdot 2 \cdot \pi \cdot 50 \cdot 300 \cdot 11} = 2{,}411.44\mu F \approx 2{,}400\mu F \quad (28)$$

This is, since SDC-CHB topology has only two capacitors, each device has approximately $1{,}200\mu F$. Thus, for this experiment, all capacitors (in CHB and SDC-CHB topologies) are equal, with $1{,}200\mu F$ individual capacitance. It is essential to note that the CHB total capacitance is six times the individual values because it has six capacitors, equal to $7{,}200\mu F$.

5.3 Results

The complete experimental results obtained on the OPAL-RT 5700 platform through signal acquisition boards and the oscilloscope are shown from Figure 5-3 to Figure 5-12, where, in each figure, the images (a) refer to CHB with $11V$ ripple (equal DC voltage ripple); the images (b) refer to CHB with $1{,}200\mu F$ individual capacitance (equal capacitance); and the images (c) refer to SDC-CHB with 11V ripple and $1{,}200\mu F$ individual capacitance. Thus, can better observe the comparisons between the results of two configurations of the classic CHB and the proposed SDC-CHB.

The system parameters used are shown in Table 5-1.

Table 5-1 - System Parameter Specifications.

Parameter	Symbol	CHB Equal Ripple	CHB Equal Capacitance	SDC-CHB
RMS grid line voltage	e_s	$400V$	$400V$	$400V$
grid frequency	f_s	$50Hz$	$50Hz$	$50Hz$
STATCOM power	S_{nom}	$\pm 25\ kVA$	$\pm 25\ kVA$	$\pm 25\ kVA$
MPC time step	T_s	-	-	$1e^{-4}s$
sampling time	T_{samp}	$5e^{-5}s$	$5e^{-5}s$	$5e^{-5}s$
carrier frequency	f_c	$2.0kHz$	$2.0kHz$	-
damping inductance	l_{damp}	$1mH$	$1mH$	$1mH$
filter inductance	l	$5mH$	$5mH$	$5mH$
filter resistance	r	$200m\Omega$	$200m\Omega$	$200m\Omega$
DC-link voltage	U_{DC}	$220V - 400V$	$220V - 400V$	$220V - 400V$
DC-link capacitance	C_{DC}	$4{,}000\mu F$	$1{,}200\mu F$	$1{,}200\mu F$
total capacitance	C_{TOT}	$24{,}000\mu F$	$7{,}200\mu F$	$2{,}400\mu F$

The oscilloscope data were imported into the Matlab software only for better graphical presentation, having not been manipulated and maintaining their originality.

The reference powers are specified to validate the proposed topology and control system strategy, maintaining a null active power, $P^*(\mathrm{k}+2)=0$, and ranging the reactive power, $Q^*(\mathrm{k}+2)$ from $-25kvar$ to $+25kvar$ to observe the converter's steady-state and dynamic performances in the same conditions.

The CHB and SDC-CHB behaviors due to reactive power variation are demonstrated in Figure 5-3, presenting in both CHB configurations higher active power ripple than in SDC-CHB, although all of them are set to $0W$ as the central value. These ripples are also observed in CHB reactive power curves when the STATCOM requires positive $Vars$, presenting a condition of difficult tuning of the classic controllers present in this topology.

The active power values include the losses in the filters and the grid connection transformer, as well as helping to regulate the DC-link capacitor voltages. The differences observed are due to the voltage waveforms generated by the different converters (SDC-CHB and CHB) are also noted in the active power curve.

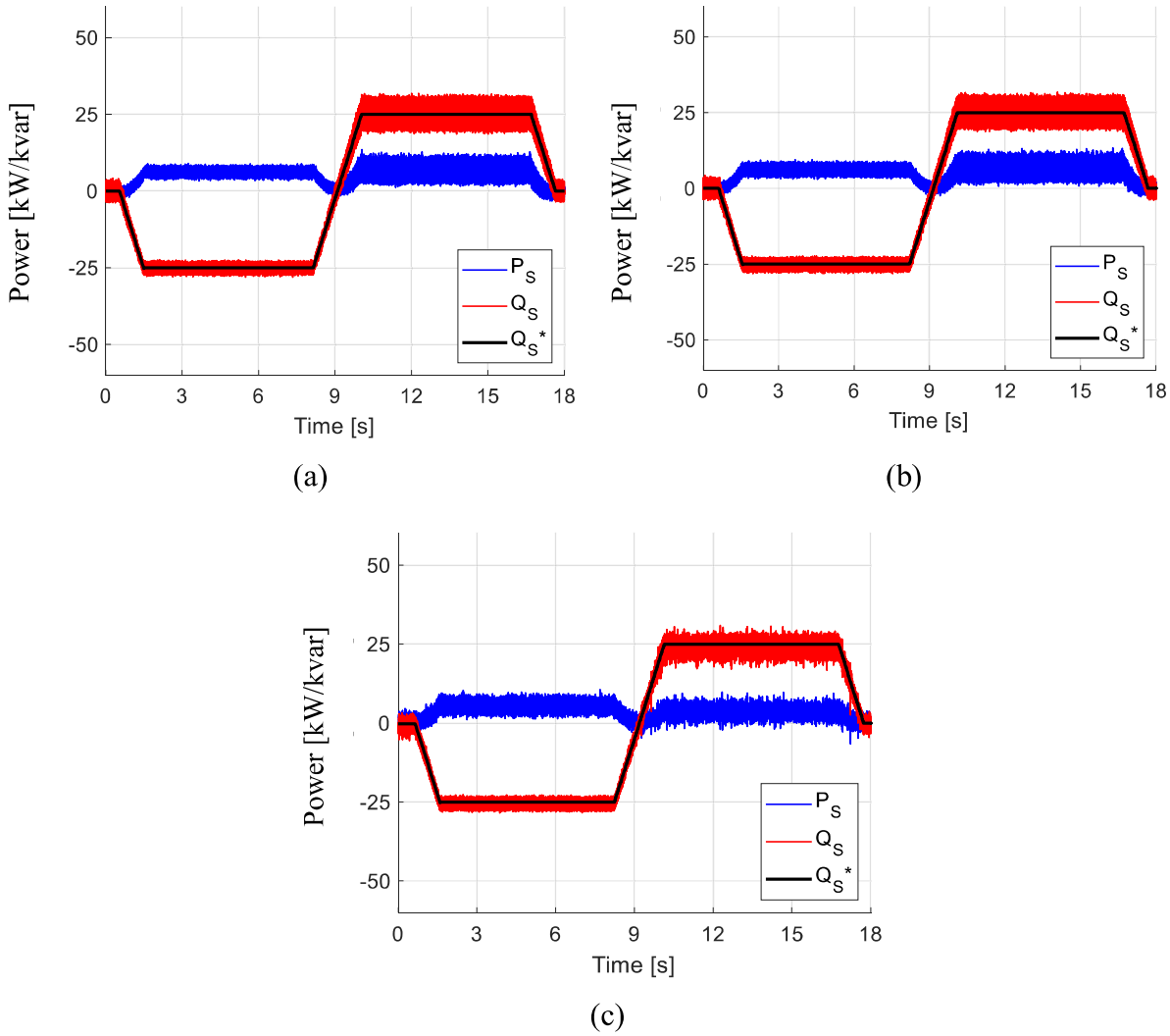


Figure 5-3– Active and reactive power: (a) CHB $(4{,}000\mu F)$; (b) CHB $(1{,}200\mu F)$; (c) SDC-CHB $(1{,}200\mu F)$ [7].

DC-link capacitor voltages analysis is one of the most critical investigation points for the converters, since their perfect operation depends on a consistent design and with adequate capacitance values, being the main topic of the comparison between the chosen topologies. Therefore, for better converters response, the reference DC-link capacitor voltages adapt to the required power, increasing or decreasing according to its variation. Therefore when the STATCOM needs to consume reactive power, the value of the DC-link voltages reduce. In contrast, when the equipment needs to provide reactive power, the DC-link voltages value rise. For no reactive power required, DC-link capacitor voltages feature $300V$; for $-25kvar$, DC-link capacitor voltages feature $220V$; and to $+25kvar$ DC-link capacitor voltages feature $380V$, as shown in Figure 5-4. This technique was used to improve the characteristics of the

harmonic spectrum of the generated wave, facilitating the flow of reactive power from the STATCOM in the different operating states.

As designed, the DC-link ripple voltage of the CHB with $4{,}000\mu F$ individual capacitance, Figure 5-4 (a), and the SDC-CHB with $1{,}200\mu F$ individual capacitance, Figure 5-4 (c), presents approximately $11V$. On the other hand, the DC-link ripple voltages of the CHB with $1{,}200\mu F$ individual capacitance, Figure 5-4 (b), presents approximately 45V.

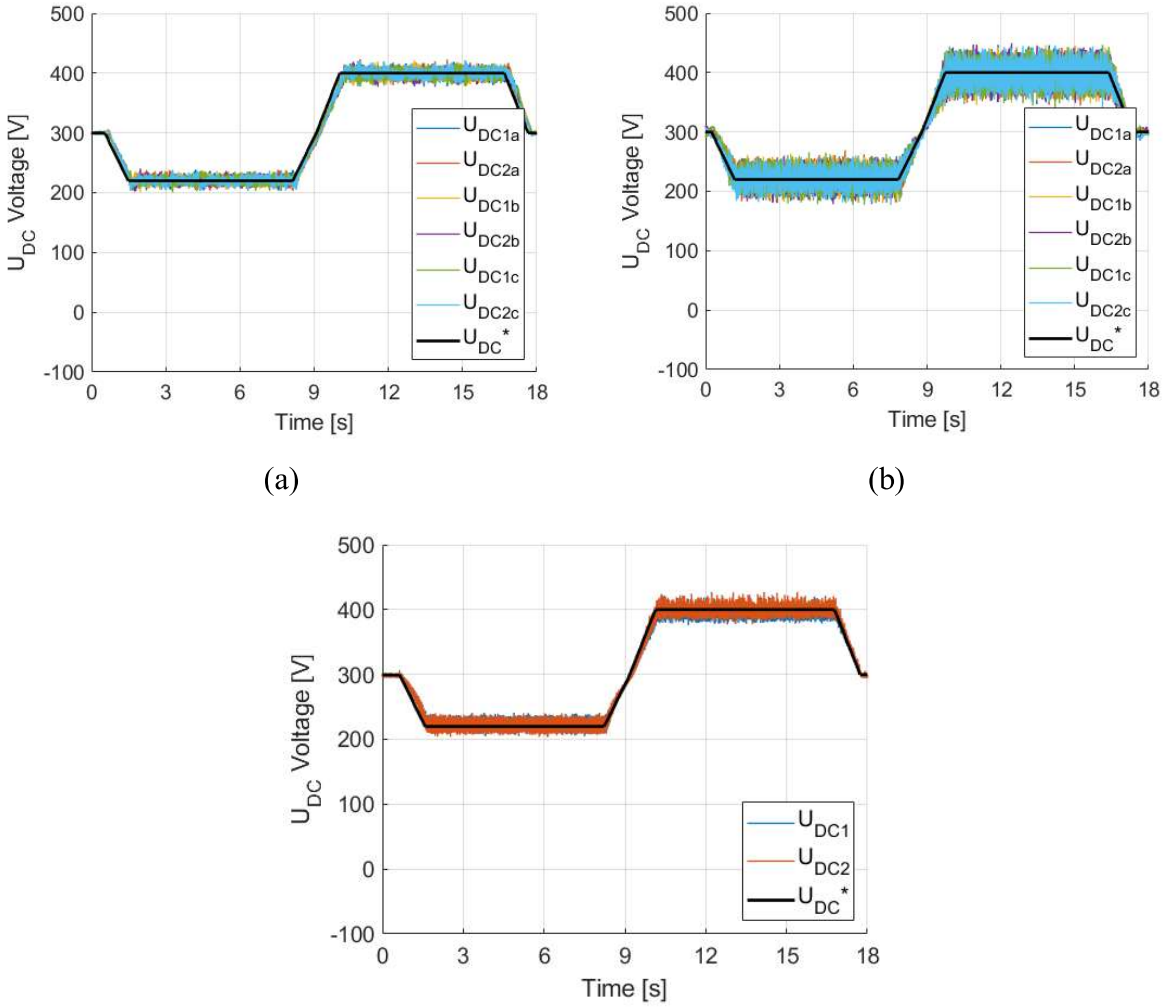


Figure 5-4– Capacitor DC-link voltages: (a) CHB (4,000µF); (b) CHB(1,200µF); (c) SDC-CHB (1,200µF) [7].

These values demonstrate in this regard the superiority of the SDC-CHB over the CHB, presenting, as previously mentioned, three times fewer capacitors and ten times less total capacitance required to obtain the same level of DC voltage ripple.

The STATCOM three-phase synthesized currents are shown in Figure 5-5 and do not exhibit significant harmonic distortions, presenting remarkable similarity among the converters and preserving its sinusoidal shape when power is required. It can be observed that the SDC-CHB currents show a high-frequency ripple higher than CHB currents due to the variable switching frequency, typical of OSV-MPC control since it is not used a PWM technique. However, the difference among the THD of topologies is numerically insignificant.

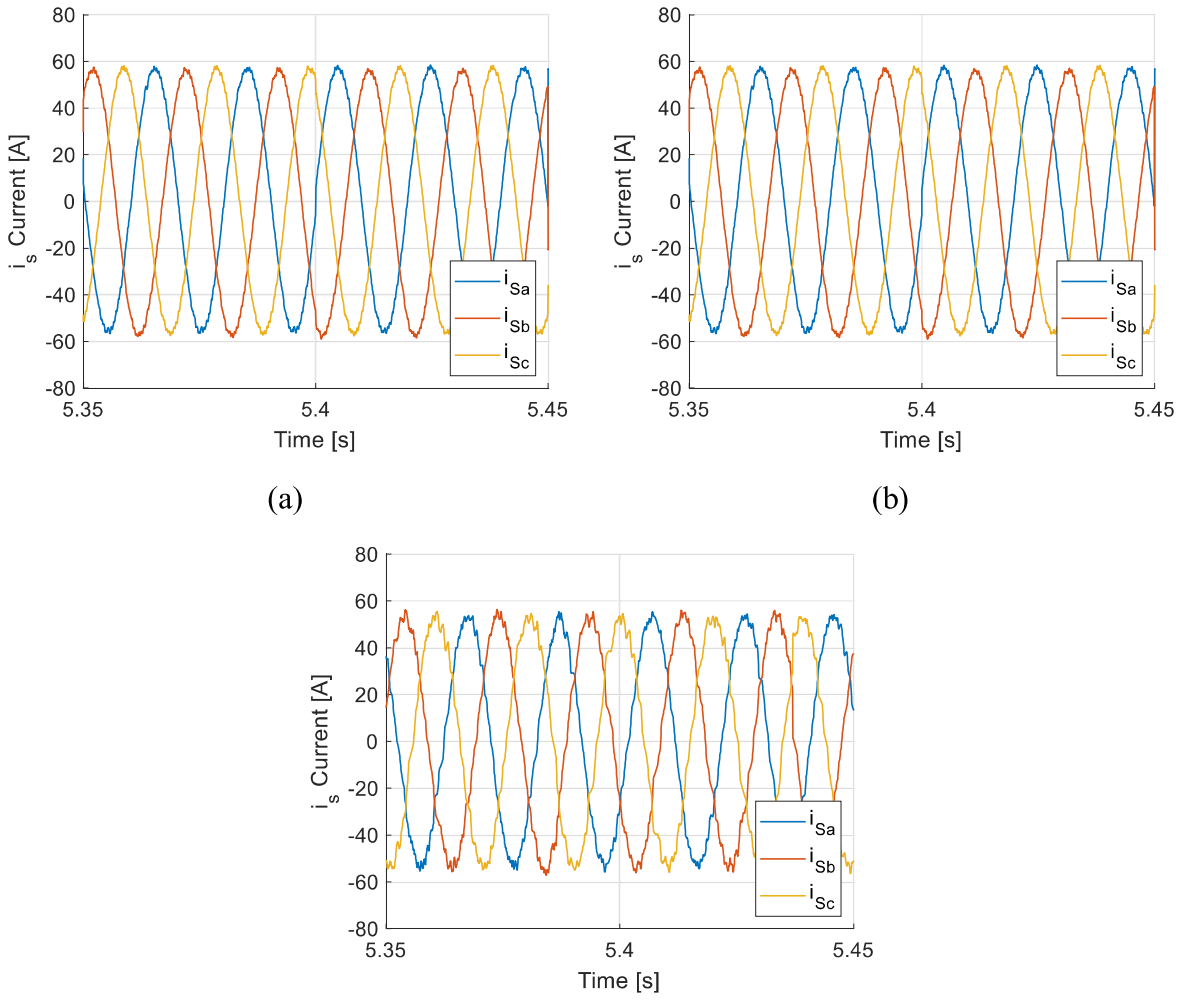


Figure 5-5– Three-phase grid currents: (a) CHB $(4{,}000\mu F)$; (b) CHB$(1{,}200\mu F)$; (c) SDC-CHB $(1{,}200\mu F)$ [7].

Figure 5-6 shows the converter's current harmonic spectrum in the inductive mode, presenting in both CHB implementations concentration close to the carrier frequency and, in the SDC-CHB close to $2kHz$. It is important to note the similarity between the frequency spectrum of the two topologies even though the MPC does not have a fixed switching frequency.

The small difference in amplitude of the fundamental wave may have been caused due to the switching characteristics of the OSV-MPC, which does not guarantee uniformity in the current ripples and in its switching frequency.

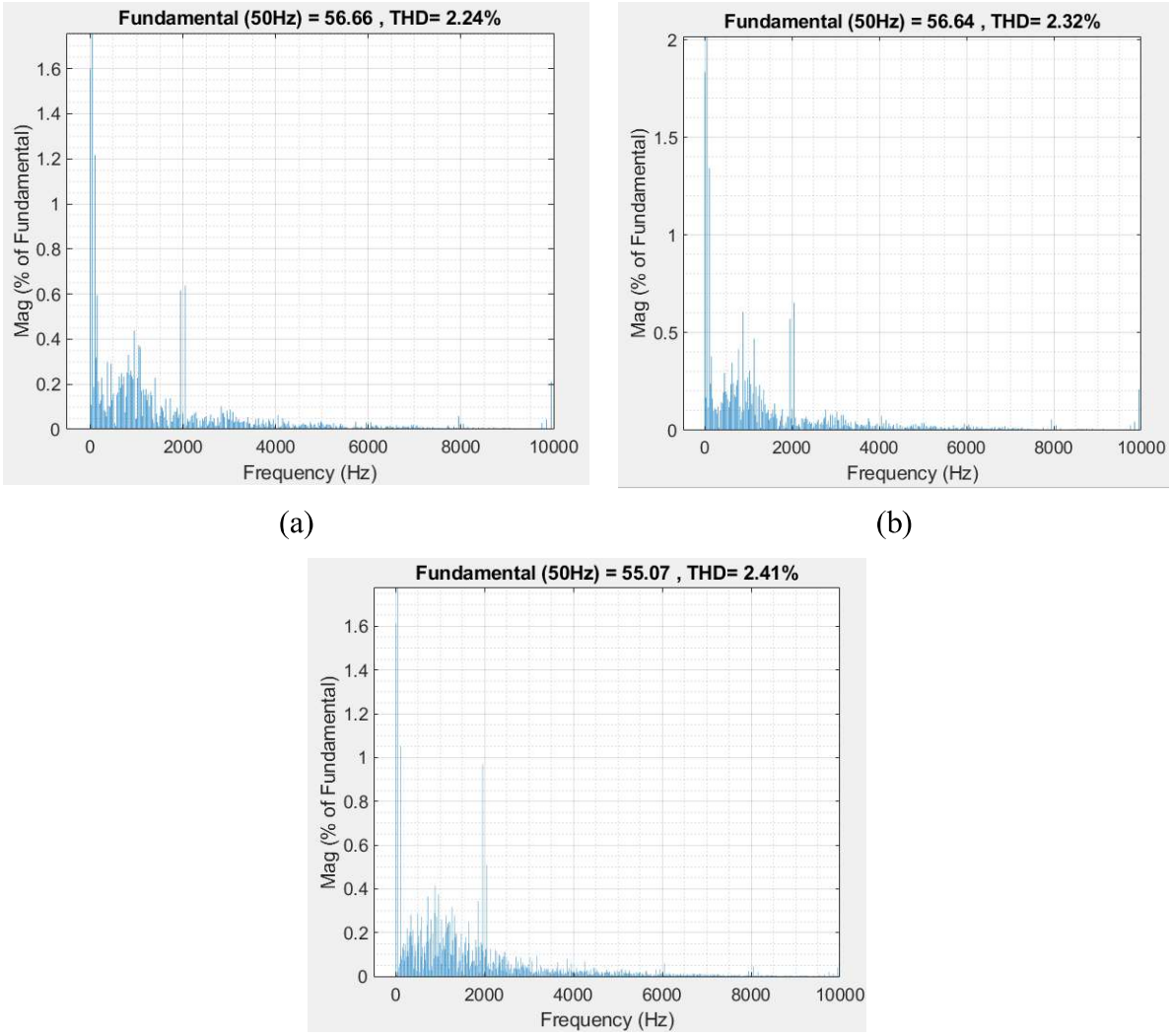


Figure 5-6– Grid current harmonic spectrum in inductive mode: (a) CHB ($4{,}000\mu F$); (b) CHB ($1{,}200\mu F$); (c) SDC-CHB ($1{,}200\mu F$) [7].

When the STATCOM is in inductive mode, requiring reactive power, the synthesized current lags the grid voltage. In contrast, when the STATCOM is in capacitive mode, providing reactive power, the current leads the voltage. This behavior can be noted in Figure 5-7 and Figure 5-8, where only the phase a voltage and current are presented. The THD values are shown in Table 3.

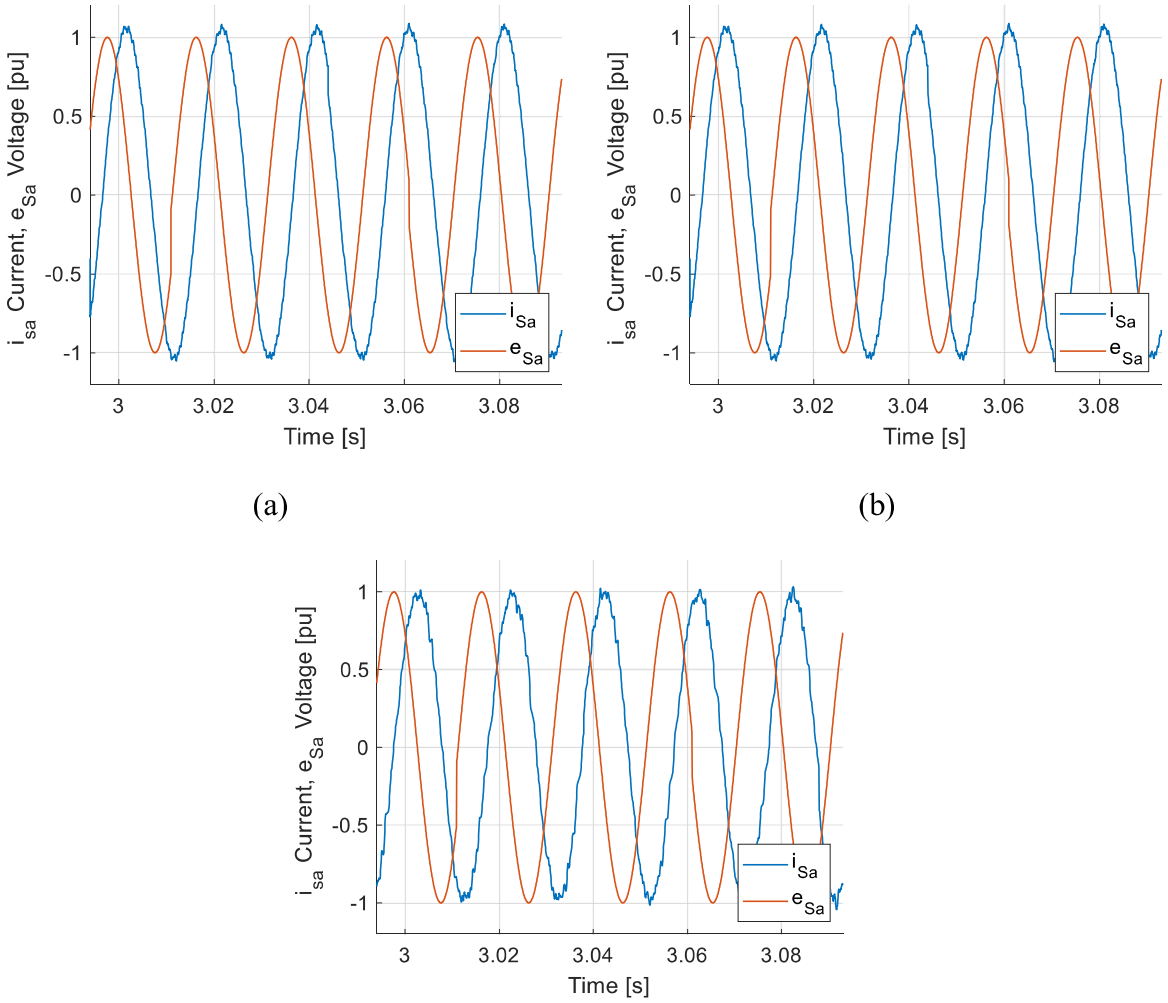


Figure 5-7– One phase grid current in inductive mode: (a) CHB $(4{,}000\mu F)$; (b) CHB $(1{,}200\mu F)$; (c) SDC-CHB $(1{,}200\mu F)$ [7].

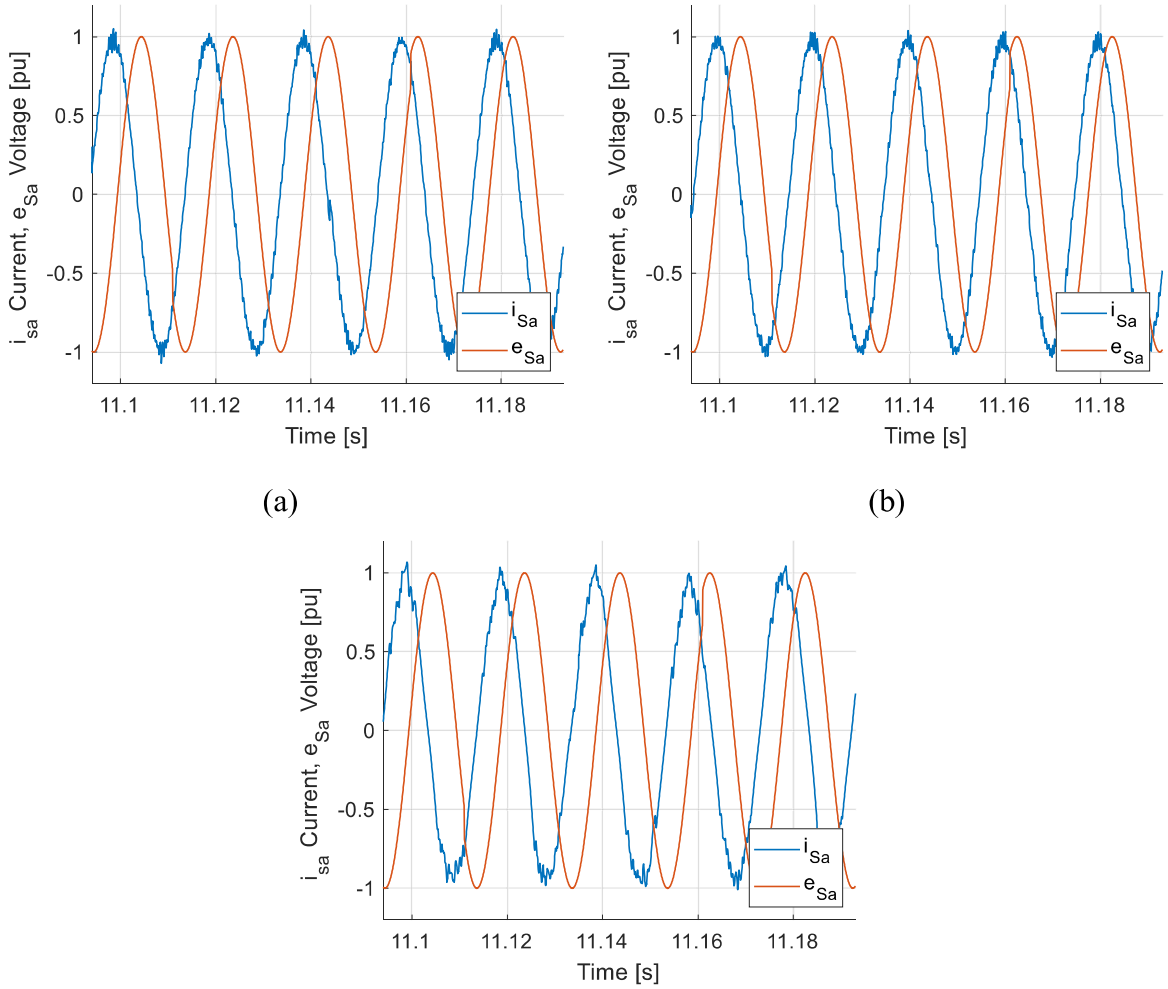


Figure 5-8– One phase grid current in capacitive mode: (a) CHB (4,000μF); (b) CHB (1,200μF); (c) SDC-CHB (1,200μF) [7].

Table 5-2 - Comparison between current Total Harmonic Distortion of topologies.

Operation mode	CHB Equal Ripple	CHB Equal Capacitors	SDC-CHB
inductive mode	2.24%	2.32%	2.41%
capacitive mode	4.08%	4.79%	4.98%

It is observed that, even with a highly reduced capacitance and having restrictions to several switching states, the SDC-CHB can provide a current waveform with little THD difference when compared with the CHB PSPWM, meeting the harmonic requirements and electromagnetic compatibility [113, 114].

Figure 5-9 shows the dynamics performance when the STATCOM reactive power shifts from inductive to capacitive modes, showing a continuous change in the current amplitude and angle about the grid voltage. This behavior corroborates with the perfect equipment functioning, presenting the possibility of operation in both situations. The MPC applied to the SDC-CHB shows agility when changing the load, presenting behavior similar to CHB using classic control, represented in the synthesized currents. Furthermore, SDC-CHB presents an automatic and fast synchronization with the grid, minimizing the power errors and showing well-defined curves.

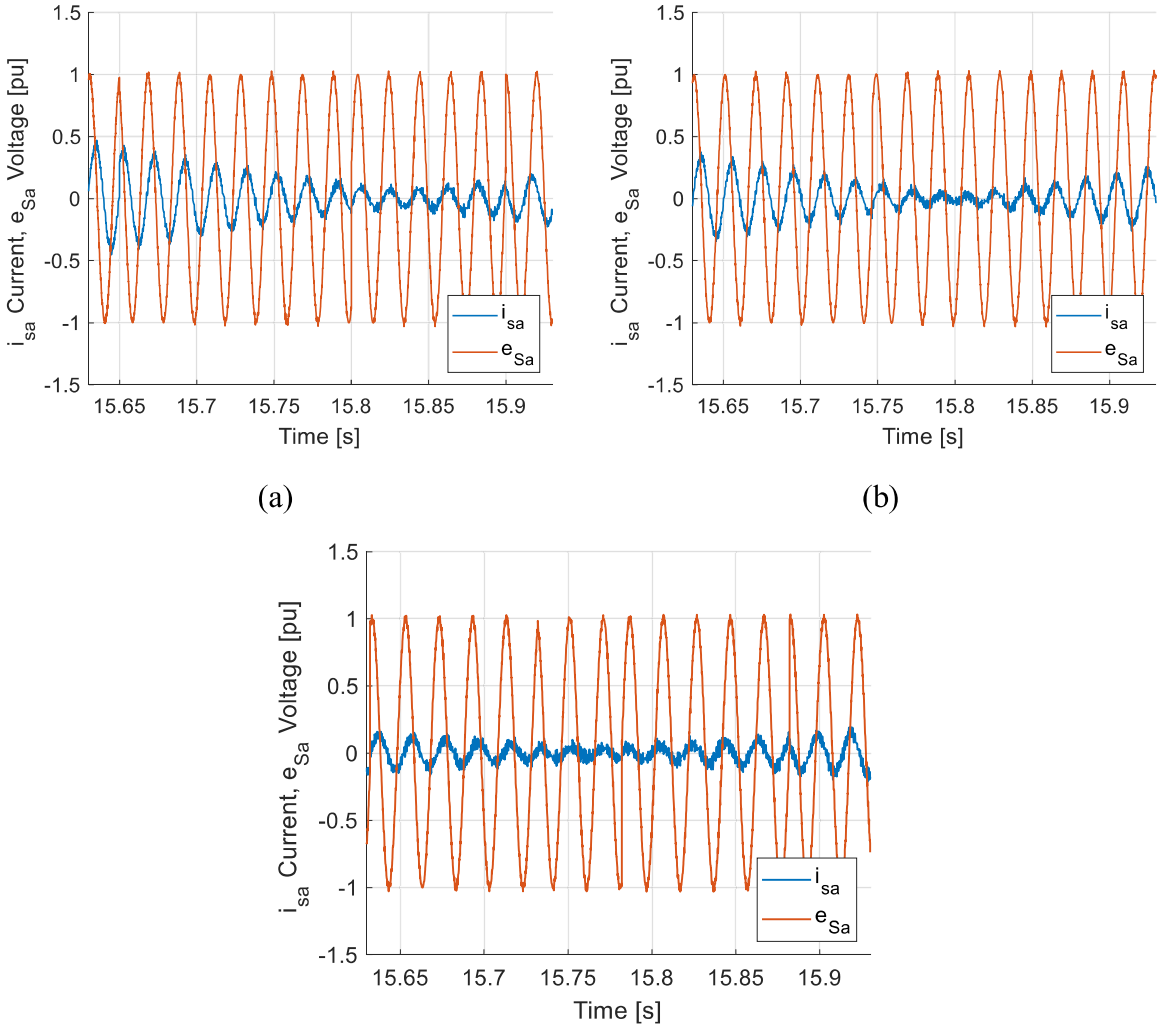
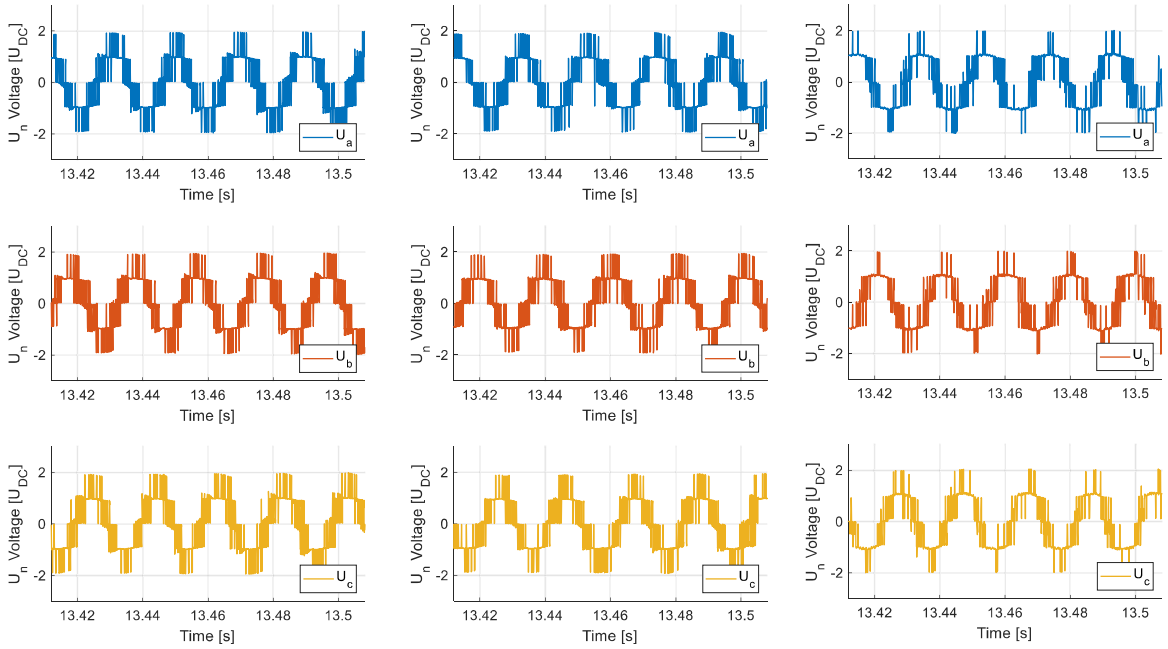


Figure 5-9– One phase grid current in changing mode: (a) CHB ($4{,}000\mu F$); (b) CHB($1{,}200\mu F$); (c) SDC-CHB ($1{,}200\mu F$) [7].

The three-phase voltage waveforms generated at the converter terminals (U_n), before the filters are shown in Figure 5-10, and the synthesized output phase-voltages can be observed.



(a) (b) (c)

Figure 5-10– Three-phase synthesized STATCOM voltage: (a) CHB ($4{,}000\mu F$); (b) CHB ($1{,}200\mu F$); (c) SDC-CHB ($1{,}200\mu F$) [7].

All the voltage waveforms have magnitude and frequency consistent with the desired specifications, with $120°$ lag among the phases as expected, and the differences resulting from each condition can be observed.

The outputs inherent to the classic CHB topology present the five voltage levels quite pronounced and well defined, presenting better results and lower the DC-link ripple. Thus, for CHB with $1{,}200uF$ individual capacitance, the oscillations present in the DC-link are higher in the voltage waveforms than those observed in the CHB with $4{,}000uF$ individual capacitance.

From another perspective, the voltage waveforms produced by the SDC-CHB with OSV-MPC present unusual waveform, with relatively fewer states in $\pm 2U_{DC}$ voltage levels.

Since the number of short circuit states surpasses 80% of possible states in this topology, the predictive control chooses, through intrinsic equations, the best switching vector that will provide the best waveform to be synthesized most similar to the desired one.

It is important to point out that the phases switching and voltage states do not coincide in a three-phase system, however, the state of the switches of each of the phases must be taken into account. For this specific five-level application, the values related to $\pm 2U_{DC}$ in each phase is the one that presents the smallest number of available possibilities.

However, it is worth mentioning that this peculiarity does not significantly affect the synthesized currents THD, presenting a slight variation among the harmonic distortion values for configurations that use CHBs with classic controls.

The voltage synthesized in each module is shown in Figure 5-11 and Figure 5-12, and presents more oscillation the smaller the DC-link. It is very pronounced in CHB with $1{,}200\mu F$ capacitors for the same reasons than previously explained in Figure 5-10, once that the sum of each module value produces the phase voltages.

The SDC-CHB presents small oscillations, and the switching pattern is less uniform than in CHB because the MPC control searches for the best module voltage value taking into account the values of other phases. This phenomenon also has little influence on the current THD.

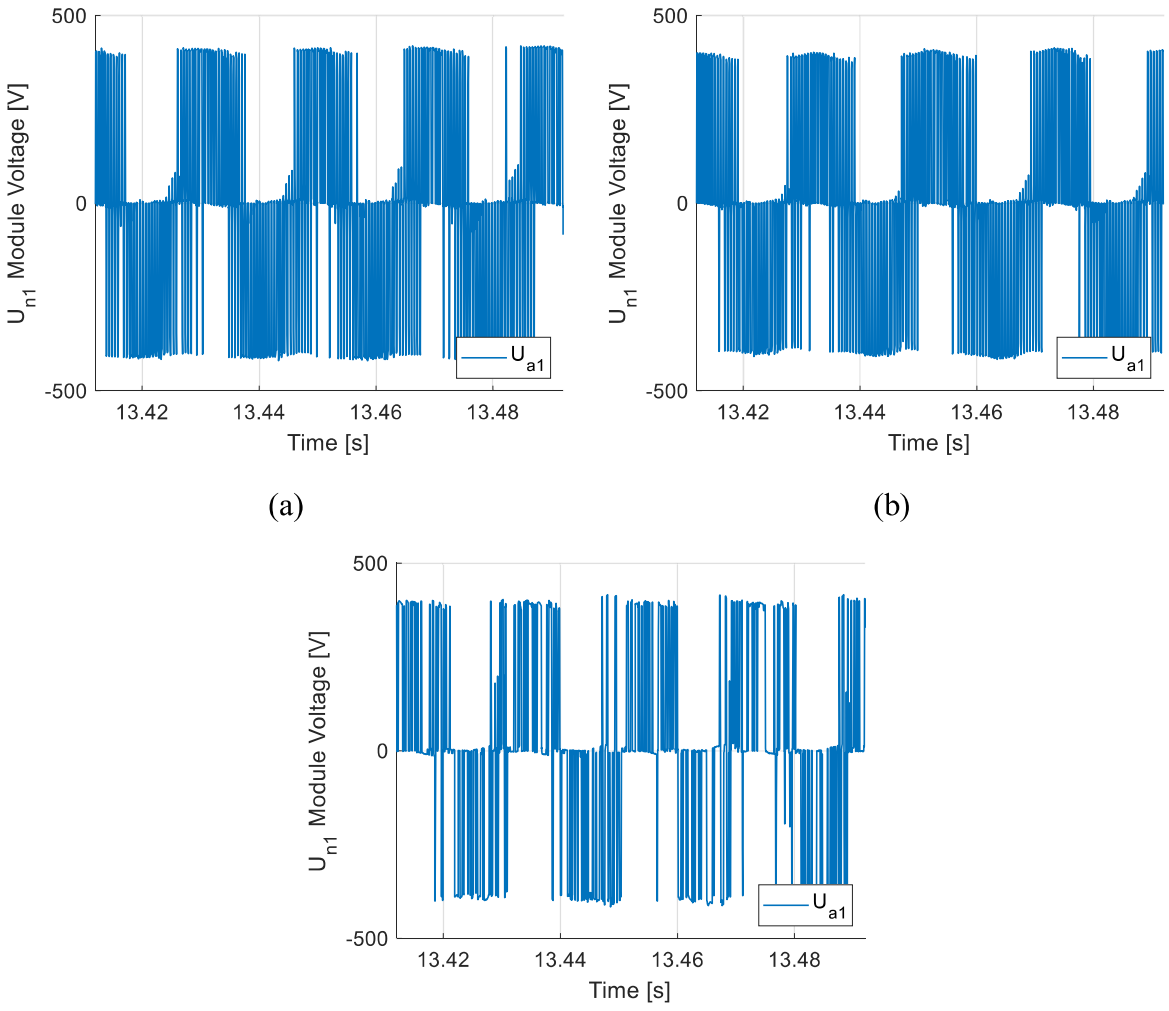


Figure 5-11– Synthesized STATCOM voltage – upper module: (a) CHB ($4{,}000\mu F$); (b) CHB ($1{,}200\mu F$); (c) SDC-CHB ($1{,}200\mu F$) [7].

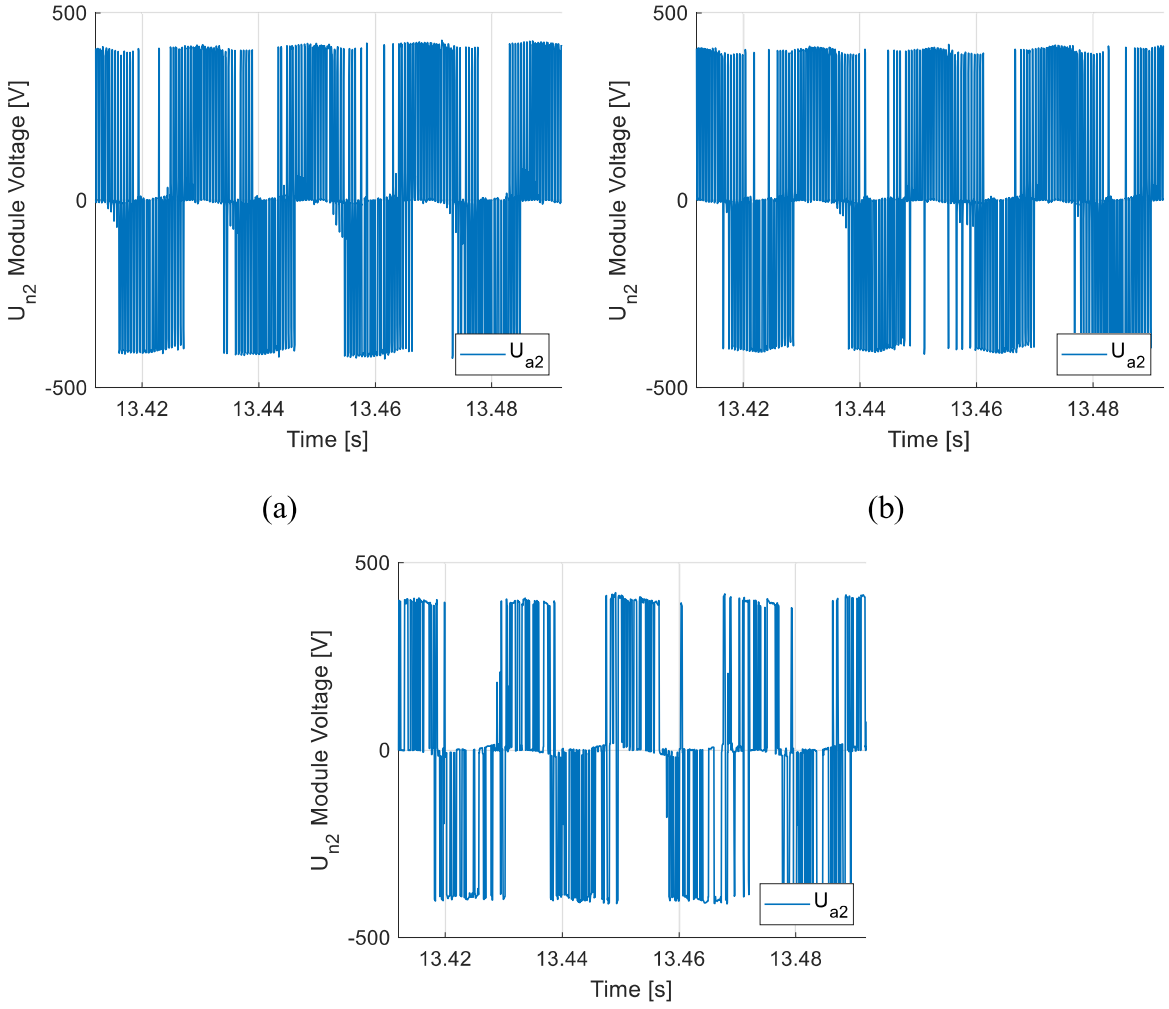


Figure 5-12– Synthesized STATCOM voltage – upper module: (a) CHB ($4{,}000\mu F$); (b) CHB ($1{,}200\mu F$); (c) SDC-CHB ($1{,}200\mu F$) [7].

5.3.1 Results explanations

The results obtained experimentally demonstrate similar operation between the two compared topologies (CHB and SDC-CHB), mainly when they operate under the same power specifications and DC-link ripple. In such a situation, the SDC-CHB has ten times less capacitance than the classic CHB.

Also, the proposed converter's three-phase structure, compared to the CHB's single-phase structure drastically and naturally reduces the oscillations in the DC-links, providing quite ease control implementation via software.

This control, which in CHB features 15 classic controllers and 6 signal low-pass filters to suit an application with five voltage levels, requires a clustered balancing control between the phases and individual balancing control between the two cascaded converters inside each cluster per phase. The tuning of all these gains becomes complex, spending a great deal of time. Furthermore, the individual balance control does not work when the reactive power reference is zero, imposing a practical limitation [108].

The SDC-CHB control does not even have an integral proportional controller, directly receiving voltage, current, and reference signals, and choosing the best switching state only via software, presenting swift responses to required power variations. Its adaptation is fast and straightforward. The comparison between topologies is shown in Table 5-3.

Table 5-3 - Comparison between five voltage levels topologies.

	CHB Same Ripple	**CHB Same Capacitors**	**SDC-CHB**
number of components	30	30	26
number of capacitors	6	*6*	*2*
individual capacitance	$4{,}000\mu F$	$1{,}200\mu F$	$1{,}200\mu F$
total capacitance	$24{,}000\mu F$	$7{,}200\mu F$	$2{,}400\mu F$
structure	single-phase	single-phase	three-phase
2ω ripple	yes	yes	no
amplitude ripple	$11V$ (3.67%)	$46V$ (15.33%)	$11V$ (3.67%)
low-pass filters	6	6	0
control elements	15	15	0
THD inductive mode	2.24%	2.32%	2.41%
THD capacitive mode	4.08%	4.79%	4.98%

The choice of the reactive power reference standards with variation in the capacitor DC-link voltages were intended to observe the SDC-CHB functioning using OSV-MPC during rapid variations of the reference signals and to analyze the ability to deal with the present transients in the systems, presenting a fast and adequate response as expected.

The thesis aims to present a new topology, show one of its applications and demonstrate the possibility of controlling it by switching strategies different from conventional PWM. Complex fault detection strategies were not added to the MPC, being the generation of references produced through calculations from instantaneous power theory and the use of a reduced time step, fast and effective enough to satisfy the objectives of this thesis. According

to the literature, MPC-based controls are used to provide better responses than some controls of the AFTC (Active fault-tolerant controller) and PFTC (passive fault-tolerant controller) type [23, 115, 116].

However, the structure of OSV-MPC, by not using control elements, allows the implementation of more elaborate failure detection controls (FTC), some of which are used in other branches of electronics, opening a vast field of studies related to these topics [117, 118].

5.4 Switching and Conductive Losses

An important analysis to be developed for devices based on power electronics refers to their switching and conduction losses, which allows estimating and calculating the equipment's performance when in use.

For the proposed SDC-CHB, the study of such losses was carried out using the PLECS® Plexim software, operating along with the Simulink Matlab® software. The analysis of thermal losses was based on models and libraries available in PLECS, which require energy dissipation based on tables and graphics present in datasheets of semiconductor switches and diodes available by manufacturers.

According to the simulations and implementations, STATCOM was able to synthesize a voltage waveform of $\pm 800V$ ($\pm 2U_{DC}$), in addition to the capacitor's DC-link ripple. A maximum current of approximately $50A$ peak was also observed.

Thus, considering the options available on the market and in the PLECS libraries, the values obtained in the experimental results, in addition to the possible transient effects, were chosen the IGBT semiconductor switches model DIM400DDS12-A000 from the DYNEX manufacturer, which supports nominal $1200V$ and $400A$ [119]. Typical switching energy curves found in the datasheet refer to 25°C ambient temperature, which is used in the simulation for switching loss analysis.

Therefore, Figure 5-13 shows two curves: switching and conductivity instantaneous losses of the converter; switching and conductivity losses of the converter through a 50 time-step moving average to smooth the curve. Both figures were generated to better represent the behavior under the effect of switching and to present more clearly the average watts consumption of the semiconductor switches in each operation mode. It should be noted that such values refer to the total consumption of STATCOM's semiconductors.

Figure 5-13 also shows the comparison of switching losses and conductivity between CHB STATCOM and SDC-CHB-STATCOM under the same reactive power requirements. The results show a small difference between those shown between Figure 5-13 and Figure 5-3, since for the analysis of switching losses and conductivity were not taken question the filters and the power grid connection transformer.

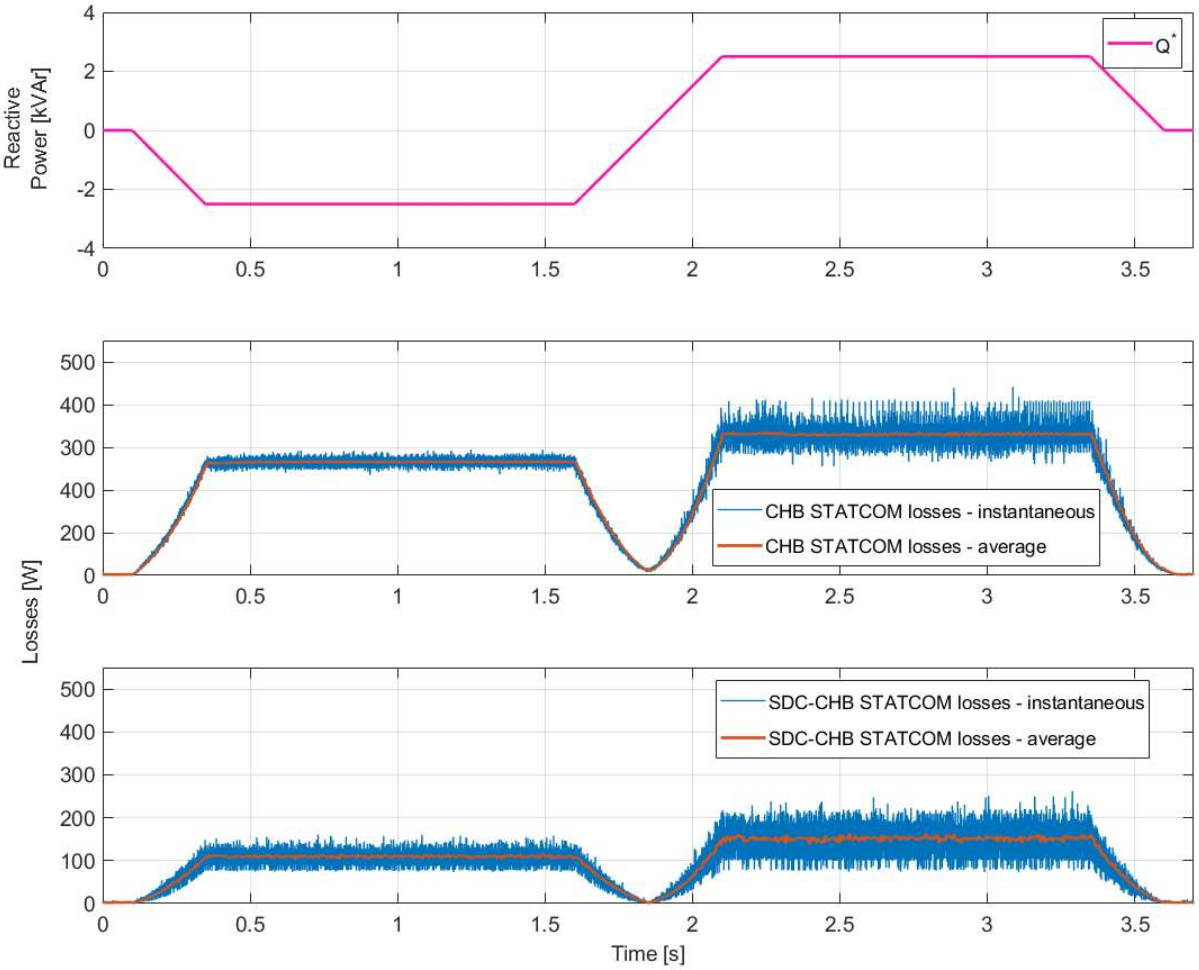


Figure 5-13– CHB STATCOM and SDC-CHB STATCOM losses.

Thus, it is observed that during the time interval in which the SDC-CHB STATCOM was operating with an inductive power factor, consuming reactive power from the electrical grid, the converter presented approximately $110W$ of thermal losses. When the device was operating with a capacitive power factor, that is, providing reactive power to the grid, it presented a consumption of approximately $150W$.

The difference in such values refers to the average voltage values applied by the converter and its relation with the grid voltage, presenting a higher or lower voltage over the

semiconductor switches to regulate the power flux. Thereby, despite the currents having the same amplitude, the thermal losses in the components present different values depending on the operating mode.

Observing the CHB STATCOM curves, it can be noted that the losses in this topology have higher values concerning the SDC-CHB STATCOM, caused by the greater number of semiconductor switches under load current regime since half of the SDC-CHB STATCOM switches are mainly used for voltage balance between modules, as shown in Figure 4-9.

Switching and conductivity losses reach a maximum of $150W$ in capacitive mode operation on the SDC-CHB STATCOM and $330W$ on the CHB-STATCOM. As the devices operate with reactive power in the $\pm 25kVAr$ range, their losses are around 1%. Therefore, according to (29) and (30), where S_{TOT} is the total STATCOM power and the $Losses$ is the absolute switching and conductive losses, the converter percentage losses are shown below.

$$\eta_{SDC-CHB} = \left(\frac{Losses_{SDC-CHB}}{S_{TOT}}\right) \times 100\% = \left(\frac{150}{25 \cdot 10^3}\right) \times 100\% \quad (29)$$

$$\eta_{SDC-CHB} = (0.006) \times 100\% = 0.6\%$$

$$\eta_{CHB} = \left(\frac{Losses_{CHB}}{S_{TOT}}\right) \times 100\% = \left(\frac{330}{25 \cdot 10^3}\right) \times 100\% \quad (30)$$

$$\eta_{CHB} = (0.0132) \times 100\% = 1.32\%$$

Table 5-4 presents numerically the conductivity and switching losses of the two STATCOMS under the same reactive power requirement, as well as the percentage difference between the values obtained about the semiconductor components.

Table 5-4 - Comparison between CHB STATCOM and SDC-CHB STATCOM losses.

	Inductive mode Losses	**Capacitive mode Losses**
CHB STATCOM	$266W$ (1.06%)	$330W$ (1.32%)
SDC-CHB STATCOM	$110W$ (0.44%)	$150W$ (0.6%)
Difference/Variation	$\mathbf{156W}$ $(\mathbf{-58,6}\%)$	$\mathbf{180W}$ $(\mathbf{-45.5}\%)$

Through the method used to determine the switching and conductivity losses, it can be observed that the CHB-STATCOM showed $330\ W$ maximum losses or 1.32%. In contrast, the SDC-CHB STATCOM had $150W$ maximum losses or 0.6%. That is approximately 45% savings compared to CHB-STATCOM.

Regarding conductivity and switching losses, STATCOM based on the proposed SDC-CHB topology using MPC has excellent performance, with low thermal losses, being competitive in this regard.

Chapter 6: Conclusions

This thesis presented a new topology proposal for power converters as a classical CHB upgrade with potential applications in various equipment to be studied and developed, using a STATCOM as an application example.

SDC-CHB topology would not have been possible to implement a few decades ago due to the various short-circuit states inherent to the use of the known PWM switching strategies. However, as actual processors can perform various calculations in tiny time intervals, a model-based predictive control strategy could be used with a full scan to provide only safe switching states, mapped using an offline mathematical tool based on the Graph Theory.

The technique developed in this thesis using Graph Theory for mapping valid switching states of converters represents topologies with short-circuit issues the viability in a vast number of applications that formerly required isolation stages or the use of low switching frequencies to operate. The contribution of this study to the branch of power electronics provided the production of several works in international events and inspired related themes of a master's dissertation, proving its usefulness and importance [60, 22, 56, 11, 16, 120, 121, 122].

The results obtained by the study and investigation of the proposed topology proved to be attractive and, following the theory involved, presenting fast response for power variations, as well as the DC-link capacitor voltage control, being developed totally in MPC platform.

The comparisons between the SDC-CHB and two different CHB configurations using classical control demonstrate the superiority of the proposed topology with MPC over the CHB used nowadays, besides obtaining undeniable SDC-CHB structural advantages.

The STATCOM experimental implementation on the HIL platform became necessary to prove the real execution of the SDC-CHB with the control and drive equipment available on the market. The results obtained using the OPAL-RT 5700 equipment present the perfect functioning of the SDC-CHB as STATCOM, showing remarkably similar and consistent results with those generated by CHBs with classic control based on similar projects with the same power and ripple on the capacitors DC-links.

The main advantages of the SDC-CHB topology over the CHB topology refer to the construction costs and the ease of controlling the parameters inherent to the project since SDC-CHB presents ten times less capacitance and three times fewer capacitor devices than the same power and ripple CHB specifications. Due to its three-phase structure, the SDC-CHB also

does not present 2ω oscillations in the capacitor voltages as observed in the classic CHB, which has single-phase structures.

Added to such features is the ease in the regulation of DC-link voltages due to its three-phase structure, being developed entirety via MPC with few code lines, against the 15 controllers necessary for the same control in the classic CHB topology, making it extremely difficult to tune the proportional and integral gains and the low-pass filters time constants.

Despite also having weight adjustments in its cost function, their tuning is simpler and requires less time from the designer. Despite its importance, the computational effort was not measured for comparison purposes.

Considering the structural analysis and the results obtained experimentally, we can conclude that the SDC-CHB topology presents itself as a modern classic CHB upgrade, having lower cost and less complexity of construction and control.

When combining the study of the switching state using Graph Theory with the OSV-MPC strategy, it was possible to propose an SDC-CHB structure that was previously unfeasible due to a large number of short-circuit states. The use of powerful processors developed and popularized in recent years, become this topology competitive in structural and operational aspects, obtaining results compatible with topologies that operate with PWM switching. Even operating with less than 1/6 (16%) of valid combinations of its semiconductor switches, the OSV-MPC presents results compatible with topologies that operate with PWM switching.

In addition, the analysis of the conductivity and switching losses of the topology applied to STATCOM demonstrate excellent consumption results, presenting values close to 0.6%, saving about 45% of energy compared to CHB STATCOM, and enabling the converter for more in-depth studies about its economic viability.

6.1 Future Works

This Thesis paved the way for a multitude of applications in energy converter devices and new approaches in power electronics. For these reasons, several fields of research and future work are available, mainly in the field of energy, many of which are already under investigation.

The future works perspective for power electronics and energy systems are listed below:

- development of switching strategies based on MPC to use SDC-CHB in fixed switching frequency;

- applications of SDC-CHB in real scenarios, such as reactive compensation, voltage control, and fault attenuation in wind systems (published work on the subject, however lacking further studies);
- development of SDC-CHB with a greater number of modules and voltage levels, which implies more complex analysis both in the study of short-circuit states and in the implementation of new predictive control;
- deepening the study of graph theory to make feasible, in addition to a greater amount of voltage levels in SDC-CHB, the development of new converters, and applications with this philosophy, such as SSTs, UPQCs, active filters, among others;
- development of devices that allow the activation of motors and other loads based on converters currently requiring isolation stages, such as CHB-B2B;
- development of a quasi-industrial platform focused on modularity and fault tolerance.

Academic Production

During the Ph.D., the path taken to develop this thesis was supported by the submission and publication of several works in events and journals, listed below:

★ Represents magazines or journals.

i. Patents

1. **Camargo, R.S.**; Encarnação, L.F.; Bueno, E.J., "*Conversor Multinível Trifásico em Cascata com Topologia Baseada em Células Trifásicas*". 2021, INPI - Instituto Nacional da Propriedade Industrial
   Deposit date: August, 23, 2021
   Patent Number: BR1020210166355

ii. Published Papers

1. Campos, B. F. A.; **Camargo, R.S.**; Bueno, E.J.; Encarnação, L.F. "Proportional Integral Model Predictive Control for a Back-to-Back Converter Based UPS". 2021 14th IEEE International Conference on Industry Applications - INDUSCON 2021, São Paulo, August 16-18 .
   https://doi.org/10.1109/INDUSCON51756.2021.9529494
   https://ieeexplore.ieee.org/document/95294940

2. ★ Bessa, A. R.; Morosini, I. C.; Encarnação, L.F.; **Camargo, R.S.**,"*Modelagem de uma Máquina Síncrona no Software de Transitórios Eletromagnéticos PSCAD/EMTDC"*. O SETOR ELÉTRICO. , v.16, p.46-50 - 50, 2021.
   https://issuu.com/revistaosetoreletrico/docs/edicao_179_final_simples_1_

3. Campos, B. F. A.; **Camargo, R.S.**; Bueno, E.J.; Encarnação, L.F. "Single-Phase AC/AC Multilevel H-Bridge Transformerless Converter with SST Functionalities". 2021 IEEE 15th International Conference in Compatibility, Power Electronics and Power Engineering - IEEE CPE-POWERENG 2021, Florence, 14-16 July 2021.
   https://doi.org/10.1109/cpe-powereng50821.2021.9501201
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4. **Camargo, R.S.**; Bueno, E.J.; Encarnação, L.F. "Asymmetric Single DC-Link Multilevel Converter with Model Predictive Control". 2021 IEEE 15th International Conference in Compatibility, Power Electronics and Power Engineering - IEEE CPE-POWERENG 2021, Florence, 14-16 July 2021
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5. ★ **R.S. Camargo,** A.E.A. Amorim, E.J. Bueno, L.F. Encarnação, "Novel Multilevel STATCOM for Power System Stability Enhancement on DFIG-Based Wind Farms". Electric Power Systems Research, Volume 197, 2021, ISSN 0378-7796. https://doi.org/10.1016/j.epsr.2021.107316.
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6. V. M. R. de Oliveira, **R. S. Camargo,** E. J. B. Peña and L. F. Encarnação, "Transformeless Cascaded H-Bridge Back-to-Back Converter Driving an Dynamic Load," *2020 IEEE PES Innovative Smart Grid Technologies Europe (ISGT-Europe)*, The Hague, Netherlands, 2020, pp. 136-140, doi: 10.1109/ISGT-Europe47291.2020.9248856.
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7. **R. S. Camargo,** D. S. Mayor, L. D. M. Fernandes, A. M. Miguel, E. J. B. Peña and L. F. Encarnação, "Non-Isolated Cascaded Multilevel Converter Based on Three-Phase Cells," *2020 IEEE PES Innovative Smart Grid Technologies Europe (ISGT-Europe)*, The Hague, Netherlands, 2020, pp. 131-135, doi: 10.1109/ISGT-Europe47291.2020.9248830.
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8. ★ **Camargo, R.S.**; Mayor, D.S.; Miguel, A.M.; Bueno, E.J.; Encarnação, L.F. A Novel Cascaded Multilevel Converter Topology Based on Three-Phase Cells—CHB-SDC. Energies 2020, 13, 4789. doi: 10.3390/en13184789.
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9. **R. S. Camargo,** D. S. Mayor, A. M. Miguel, E. J. B. Peña and L. F. Encarnação, "STATCOM Real-Time Implementation Based on a NovelCascaded Multilevel Converter Topology", OPAL-RT's 12th Conference on Real-Time Simulation, ON LINE, 2020, June 18-19, 2020.
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11. **R. S. Camargo,** D. S. Mayor, L. De Mingo Fernandes, A. M. Miguel, E. J. B. Peña and L. F. Encarnação, "A Novel Cascaded Multilevel Converter Topology Based on Three-Phase Cells with Model Predictive Control," 2020 IEEE 29th International Symposium on Industrial Electronics (ISIE), Delft, Netherlands, 2020, pp. 1161-1166, doi: 10.1109/ISIE45063.2020.9152294.
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12. V. M. R. de Oliveira, **R. S. Camargo** and L. F. Encarnação, "Field Oriented Predictive Current Control on NPC Driving an Induction Motor," 2020 IEEE International Conference on Industrial Technology (ICIT), Buenos Aires, Argentina, 2020, pp. 169-174, doi: 10.1109/ICIT45562.2020.9067236.
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15. **Camargo, R. S.**; Encarnacao, L. F. ; Rocha Junior, E. B., "Estudo De Modernização Do Transporte De Minério De Ferro Via Acionamento Com Inversores Multiníveis." In: 13th IEEE/IAS International Conference on Industry Applications - INDUSCON 2018, 2018, São Paulo. Estudo De Modernização Do Transporte De Minério De Ferro Via Acionamento Com Inversores Multiníveis, 2018.
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16. Rocha Junior, E. B. ; **Camargo, R. S.** ; Lopes, L. G. S. ; Batista, O. ; Savio Lyrio Simonetti, Domingos. "Dispositivos Limitadores de Corrente de Falta a Estado Sólido Utilizados Na Proteção de Sistemas de Distribuição: Revisando a Literatura Entre 2006 E 2017." In: 13th IEEE/IAS International Conference on Industry Applications - INDUSCON 2018, 2018, São Paulo.
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