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LAILA SINDRA RIBEIRO

A CONTROL STRUCTURE FOR A BIDIRECTIONAL DC-AC CONVERTER WITH POWER QUALITY SUPPORT FUNCTIONS

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Dissertation submitted to the Graduate Program in Electrical Engineering from the Technological Center of the Federal University of Espirito Santo as a partial requirement for obtaining a Master's Degree in Electrical Engineering.
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"The Lord has done great things for us, and we are glad."
(Holy Bible, Psalms 126:3 - NKJV)

Abstract

The expansion of distributed generation, especially photovoltaic, provokes an increase in the number of DC-AC converters connected to the grid. These converters may offer power grid support functions such as power factor correction and compensation of the current harmonic components. Those functions raise the equipment relevance to the grid and contribute to the power system's confiability and power quality. In this context, the objective of this work is to design a DC-AC converter with the grid support functions as power factor correction and harmonic compensation, besides electrical power interchange. The work focuses on the controller of the converter, with the algorithms embedded in a DSP and power converter in a Hardware In the Loop (HIL). This dissertation includes a theoretical background of the converter topology operation, filter design, and control loops used in the project. Experimental results demonstrate that the converter is capable of operating with grid support functions with a good performance, correcting power factor and compensating 3^{rd}, 5^{th}, and 7^{th} harmonics. Furthermore, the converter can have multiple functions activated, distributing its power capacity to prioritize the chosen operation mode.

Keywords: DC-AC converter; Power factor correction; Harmonic compensation; Distributed generation; Hardware in the loop.

Resumo

O crescimento da geração distribuída, em especial fotovoltaica provoca também o aumento do número de conversores CC-CA conectados à rede. Esses conversores podem oferecer serviços de suporte à rede como correção de fator de potência e compensação das componentes harmônicas da corrente, além da bidirecionalidade do fluxo de potência. Tais funções aumentam a relevância do equipamento para o sistema elétrico e contribuem para confiabilidade da rede e qualidade da energia. Nesse contexto, o objetivo deste trabalho é projetar um conversor CC-CA com as funções de suporte à rede de correção de fator de potência e compensação de harmônicos. O foco do trabalho é o controlador do conversor e os testes dos algoritmos, embarcados em um DSP, são feitos com experimentos do tipo *Hardware In the Loop* (HIL). Esta dissertação inclui uma revisão teórica sobre o funcionamento da topologia do conversor, projeto do filtro e sobre as malhas de controle utilizadas no trabalho. Os resultados dos experimentos demonstram que o conversor é capaz de operar com funções de suporte à rede com boa performance, corrigindo fator de potência da componente fundamental e compensando 3^o, 5^o e 7^o harmônicos. Além disso, o conversor pode operar com múltiplas funções, distribuindo sua capacidade de potência para priorizar o modo de operação escolhido.

Palavras-chave: Conversor CC-CA; Correção de fator de potência; Compensação de harmônicos; Geração Distribuída; *Hardware in the loop*.

List of Figures

List of Tables

List of abbreviations and acronyms

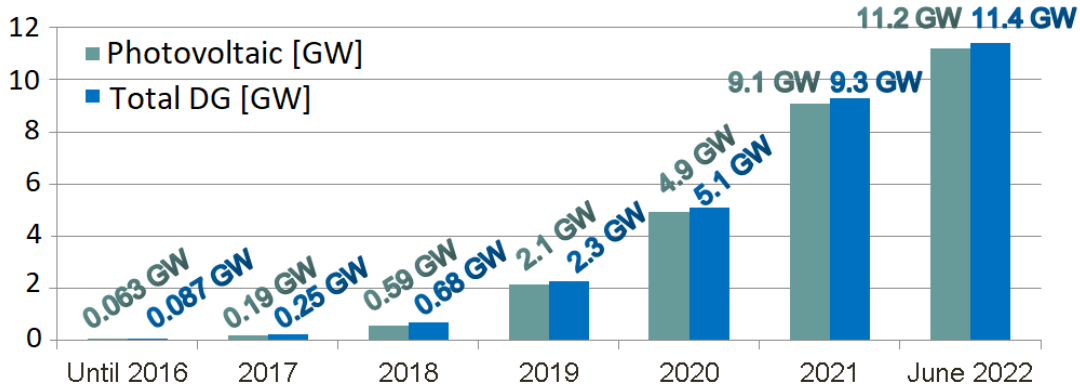
APF	Active Power Filter
BESS	Battery Energy Storage System
BMS	Battery Management System
DER	Distributed Energy Resource
DFT	Discrete-time Fourier Transform
DG	Distributed Generation
FB	Full-Bridge
FB-T	Full-Bridge T-cell
HIL	Hardware-In-the-Loop
LV	Low-Voltage
MCU	Micro-Controller Unit
NMC	Nickel Manganese Cobalt
PF	Power Factor
PICC	Proportional Integral Current Controller
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SOGI	Second-Order Generalized Integrator
STATCOM	Static Synchronous Compensator

Contents

1 Introduction

Distributed Generation (DG) has been increasing rapidly in the past decade, especially solar energy. According to EIA (2022), the world's solar electricity net generation increased from 0.3 billion kWh in 1989 to 700 billion kWh in 2019. In Brazil, this growth is also observed, with DG installed capacity rising from 0.087 GW in 2016 to 11.4 GW in June of 2022, and most DG is from photovoltaic generation (ANEEL, 2022). Figure 1 depicts Brazil's DG installed capacity per year.

Figure 1 – Installed Capacity per Year in Brazil



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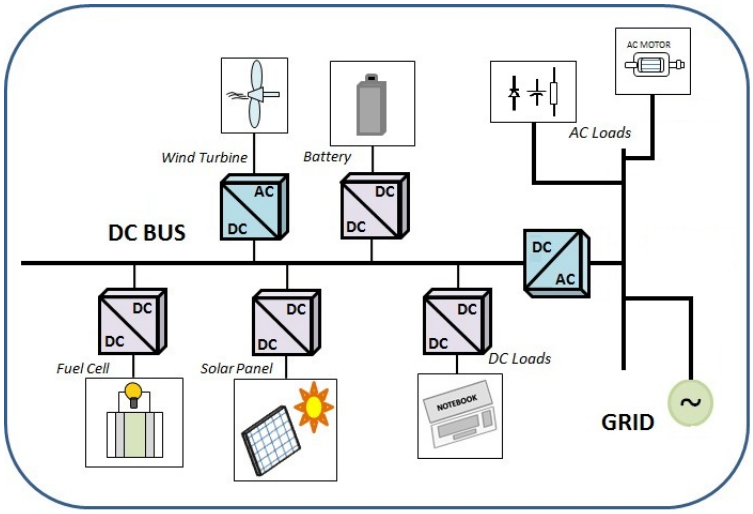
In addition to photovoltaic installations, DC microgrids are also gaining increased interest, with several works exploring control strategies and microgrids performances (Wu et al., 2014) (Balaguer et al., 2011) (Lopes; Moreira; Madureira, 2006). Lopes, Moreira and Madureira (2006) defines a microgrid as an Low-Voltage (LV) network with the network loads and several small modular generation systems connected to it. Figure 2 illustrates an example of a microgrid.

A DC-AC converter is employed to connect a DC microgrid (such as the photovoltaic DG) to the utility grid. Usually, this converter's primary function is to exchange active power. However, additional power system support functions are emerging (Xu; Xue; Chang, 2021) (Zhao et al., 2018). Some support functions are reactive power control, harmonic compensation, voltage regulation, and frequency regulation. Standards have been updated, and expect that Distributed Energy Resources (DER) provide support functions aiming to incorporate higher DER penetration and to maximize its relevance to the grid (Xu; Xue; Chang, 2021).

From the support functions aforementioned, two will be further discussed in this work: reactive power control and harmonic compensation. Reduction of reactive power

Figure 2 – A basic DC/AC microgrid



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flowing through the grid brings benefits such as diminished utility losses, improved voltage regulation, and smaller reactive current, liberating the system capacity to deliver active power. Since most consumer loads have inductive behavior, capacitors are usually employed to supply reactive power. However, capacitors cannot consume reactive power and are sources of electrical transients during connection. A solution is the use of a Static Synchronous Compensator (STATCOM). A STATCOM is defined by Hingorani and Gyugyi (2000) as a shunt-connected var compensator whose capacitive or inductive output current can be controlled independently of the AC system voltage. When the STATCOM is composed of a voltage-sourced converter, the equipment output voltage is adjusted so that the required reactive current flows into or from the AC system.

The converter also can be designed to act as an active filter for harmonic compensation to support the utility grid. Harmonic pollution in power grids can cause several problems, such as transformers and electrical motors overheating, voltage waveform distortion, and interference with communication systems (Akagi; Watanabe; Aredes, 2007). The converter's output voltage is controlled to provide or sink the harmonic current, compensating for harmonics and releasing those undesired components from the utility.

When a test bench with a converter is unavailable, or a non-destructive initial prospection is intended, real-time simulations can be used to test the physical controller for the inverter. In a Hardware-In-the-Loop (HIL) simulation, a virtual plant substitutes the real plant in a real-time simulator. The virtual plant usually costs less and allows extreme event testing (Bélanger; Venne; Paquin, 2010).

1.1 Objectives

1.1.1 General Objective

This dissertation focuses on designing a DC-AC converter with power systems support functions of reactive power control and harmonic filtering. The inverter testing is through HIL simulations.

1.1.2 Specific Objectives

Specific objectives are listed below:

- Study the inverter topology, and the generation of its adequate Pulse Width Modulation (PWM) switching signals in a microcontroller;
- Design LCL filter to connect the inverter to the grid and filter switching harmonics;
- Implement a Phase-Locked Loop (PLL) to synchronize the DC-AC converter with the main grid;
- Design a current controller for the inverter;
- Design reactive power controller for STATCOM operation;
- Implement a control strategy for harmonic filtering;
- Design battery management functions;
- Test the inverter operation through HIL simulations;

1.2 Motivation

The number of DC-AC converters connected to the grid has been increasing in the last decade, together with DG. Although today those inverters' prime function is to control active power flow, power system support functions are emerging. Those functions increase the inverters' value to the grid since they allow the DER to contribute to the grid stability and confiability, besides improving power quality. Therefore, this dissertation is motivated by those benefits that power system support functions bring to the grid.

1.3 Dissertation Structure

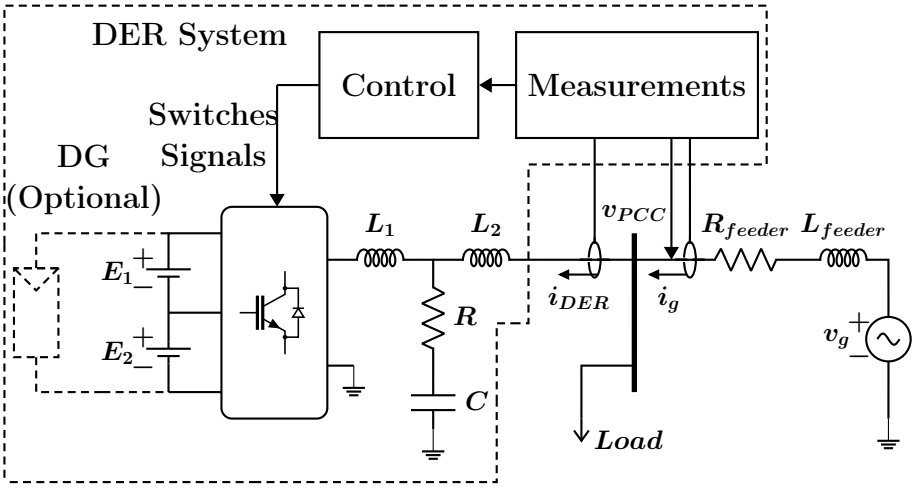
In chapter 2, the reader finds a theoretical background covering several topics necessary to design the converter, its peripherals, and the power system support functions

implemented, providing information that supports the choices made during the project development. Chapter 3 details the project, presenting the power grid simulated, the microcontroller's resources used and its configuration, parameters adopted in controllers and block diagrams, and the logic of the converter operation modes. Meanwhile, chapter 4 presents and discusses the simulations' results. Then, conclusions and future work are considered in chapter 5. Finally, the references cited are listed at the end of the document.

2 Theoretical Background

The DER system's structure and connection with the grid are displayed in Figure 3. This chapter presents a theoretical background on parts of the DER system operation: DC-AC converter chosen topology, Battery Energy Storage System (BESS), LCL filter, Phase-Locked Loop (PLL), Current Control Loop, Reactive Power Control, and Harmonic Compensation. Alternatively, the BESS can stay connected to a DC bus including DG, as seen in Figure 2.

Figure 3 – DER system



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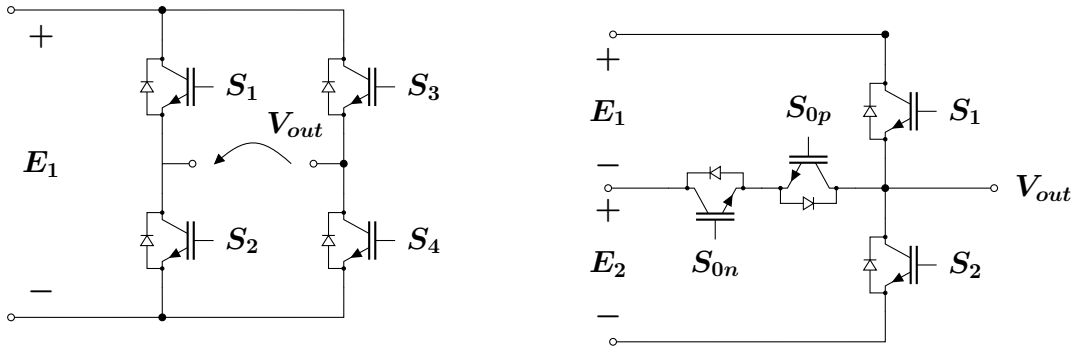
2.1 DC-AC Converter Topology

A usual single-phase topology for inverters is a Full-Bridge (FB), shown in Figure 4a. This topology output voltage can have two or three levels, according to the modulation employed. A five-level converter can be constructed by replacing one of the FB's (Figure 4a) legs with a T-cell (Figure 4b), resulting in the modified topology named Full-Bridge T-cell (FB-T), displayed in Figure 5. FB-T can produce five voltage levels and was proposed by Hinga, Ohnishi and Suzuki (1994). Although initially multilevel inverters where thought to be applied at high voltage levels, recently they are being applied also to low-voltage applications (Teichmann; Bernet, 2005) (Soeiro; Heldwein; Kolar, 2013) (Simonetti; Yuan, 2019).

Modifications of the FB-T have been studied to produce more voltage levels (Varghese; Eldhose; Joy, 2014) (Kalaiselvan, 2016) (Meenakshi; Kumar; Ramprakash, 2016). When increasing the number of levels, the inverters' output voltage tends to have

Figure 4 – Full-Bridge and T-cell Topologies



(a) Full-Bridge (b) T-cell

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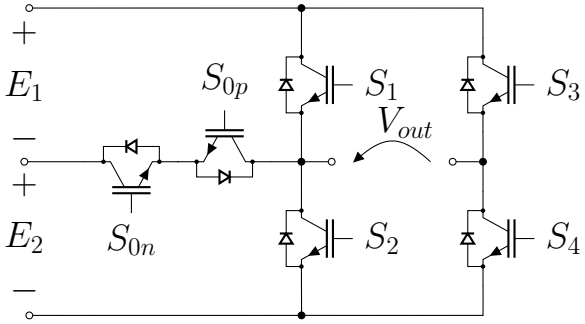
Figure 5 – Full-Bridge with T-cell converter



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less harmonic distortion. However, as the number of output voltage levels escalates, the controllers' complexity also increases. Additionally, the possibility of voltage unbalance problems arises (Rodriguez; Lai; Peng, 2002). The FB-T presents a good trade-off between complexity and levels quantity.

2.1.1 Modulation

The operation of the inverter is divided into four modes to ease its explanation, exemplified in Figure 6. In each operation mode, a pair of switches alternate to change between two voltage levels. Table 1 shows the levels alternated in each one of the modes and the switches configuration in each case; 0+ and 0− correspond to zero at the positive semi-cycle of the reference and negative semi-cycle, respectively. Three complementary PWM outputs can generate the six switches signals: S_1 is complementary to S_{0p}, S_2 is complementary to S_{0n}, and S_3 is complementary to S_4. The pair S_3S_4 switches at the grid frequency. In modes I and III, the PWM pair S_1S_{0p} are switching while the others remain at a fixed state, whereas in modes II and IV, S_2S_{0n} are switching, and the other pairs remain fixed.

Figure 6 – Output voltage example

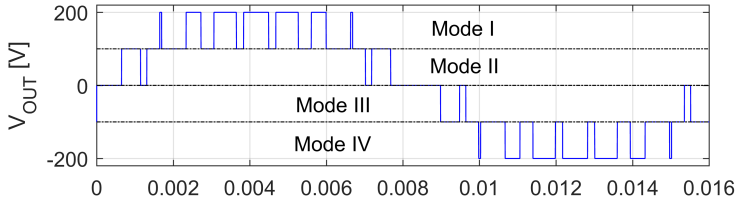

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Table 1 – Output voltage and switches states

Mode	Level	Switches					
		S_{0p}	S_{0n}	S_1	S_2	S_3	S_4
Mode I High	$E_1 + E_2$	off	on	on	off	off	on
Mode I Low	E_1	on	on	off	off	off	on
Mode II High							
Mode II Low	0+	on	off	off	on	off	on
Mode III High	0−	off	on	on	off	on	off
Mode III Low	$-E_2$	on	on	off	off	on	off
Mode IV High							
Mode IV Low	$-E_1 - E_2$	on	off	off	on	on	off

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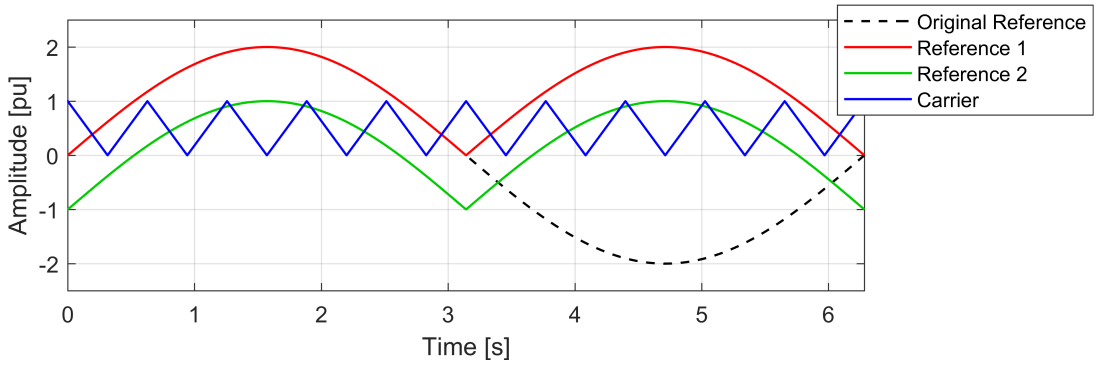
One way of modulating the inverter is with a single carrier and multiple references, as shown by Aziz and Salam (2002) in other 5-level topology. This method utilizes two references formed by the module of a sine wave, a semi-cycle indicator, and the carrier. Figure 7 depicts the disposition of the references and the carrier. When operating in the positive semi-cycle, the inverter operates in mode II if reference 2 is below zero. For this case, the voltage output is 0+ if the carrier is above reference 1 and E_1 if the carrier is below reference 1. Therefore, reference 1 drives the pair $S_2 S_{0n}$. S_2 is *on*, and S_{0n} is *off* if reference 1 is greater than the carrier. Otherwise, S_2 is *off*, and S_{0n} is *on*. When reference 2 is above zero, the inverter operates on mode I. In this case, E_1 is the voltage output if the carrier is above reference 2 and $E_1 + E_2$ otherwise. Consequently, reference 2 drives the pair $S_1 S_{0p}$. S_1 is *on*, and S_{0p} is *off* if reference 2 is above the carrier, and S_1 is *off*, and S_{0p} is *on* otherwise. For modes I and II, S_3 is *off* and S_4 is *on*. The same logic applies to modes III and IV in the negative semi-cycle.

The higher the carrier frequency, the easier it is to filter the harmonics caused by the modulation. However, a high switching frequency can increase switching losses. In addition, a dead time must be inserted to allow a switch to finish the turn off before its complementary turns on, avoiding short-circuit. Meanwhile, frequencies above 20 kHz reduce noises emitted by the inverter since this frequency is above the human hearing range.

Figure 7 – Multiple references modulation



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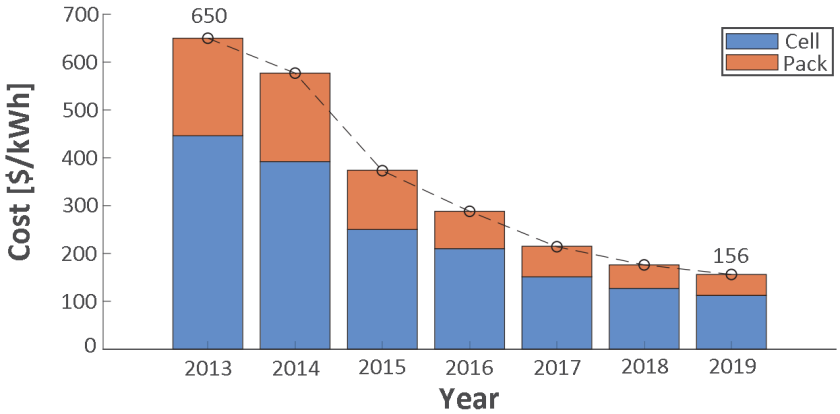
2.2 Battery Energy Storage System

The DC sources (E_1 and E_2) for the DC-AC converter are formed by battery banks. Photovoltaic installations or wind turbines are intermittent power sources. However, energy storage allows fluctuating renewable energy sources to be as stable as conventional systems (Sørensen, 2007). Lithium-ion batteries show high efficiency (over 90%), high energy density (90–190 Wh/kg), and a long lifetime (up to 10000 cycles) (Stecca et al., 2020). The performance of Lithium Nickel Manganese Cobalt (NMC) based technology has contributed to bringing about NMC as the primary Li-ion technology for stationary storage (Commission et al., 2018). Additionally, the cost of lithium batteries reduced in the last decade, as seen in Figure 8.

Figure 8 – Lithium battery costs

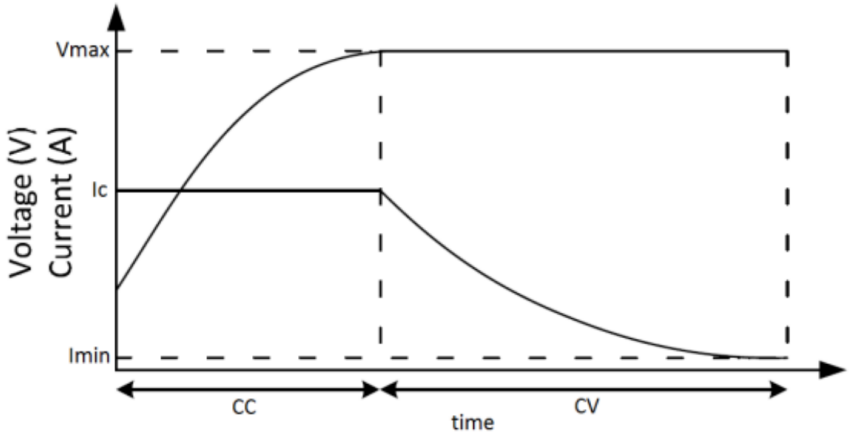


Font: Stecca et al. (2020).

Since lithium batteries are sensitive, they usually need a Battery Management System (BMS) to collect measurements, balance cells' voltage, protect them against overloading, minimize temperature gradient, and compute the state of charge and state of health (Stecca et al., 2020). Constant current constant voltage (CC-CV) is the most common lithium battery charging process because of its simplicity and ease of implementation

(Tomaszewska et al., 2019). The CC-CV method is similar to lead-acid batteries. However, lithium batteries support higher charging current and almost no over voltage, while lead-acid batteries require smaller currents and tolerate more over voltage (PS, 2022). The higher charging current of lithium batteries makes them able to charge faster when compared to lead-acid batteries. Figure 9 shows a typical charging curve when using the CC-CV method. PS (2022) recommends choosing I_c of 0.5C, where C is the battery capacity, V_{max} of up to 15 V for a 12.8 V rated battery pack, and I_{min} of 0.03C. The DC-AC converter control system implements this charging process to charge the battery bank when necessary.

Figure 9 – CC-CV typical charging curve



Font: Amin, Ismail and Hapid (2018).

2.3 LCL Filter

The LCL filter consists of two inductors in series and a capacitor in parallel between the inductors. Its function is to filter high-order harmonics generated by the DC-AC converter. Figure 10 depicts the scheme for this filter. The strategy proposed by Reznik et al. (2014) was used to design values for inductance, capacitance, and resistance. A similar method was also employed by Liserre, Blaabjerg and Hansen (2005). A flowchart summarizing the design strategy is shown in Figure 11.

The information required to design the filter is the converters' rated power S_b, grid frequency f, switching frequency f_{SW}, DC source voltage V_{DC}, and the grid nominal RMS voltage $V_{g\ RMS}$. With these values, the inverter's base impedance Z_b and base capacitance can be calculated with equations 2.1 and 2.2, respectively.

$$Z_b = \frac{V_{g\ RMS}^2}{S_b} \tag{2.1}$$

$$C_b = \frac{1}{2\pi f Z_b} \tag{2.2}$$

Figure 10 – LCL filter

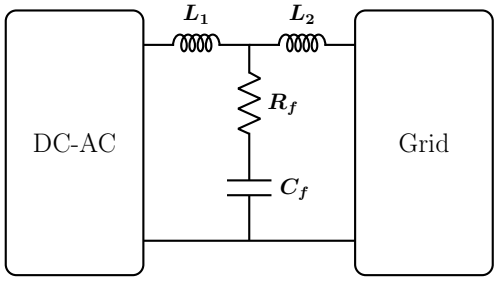


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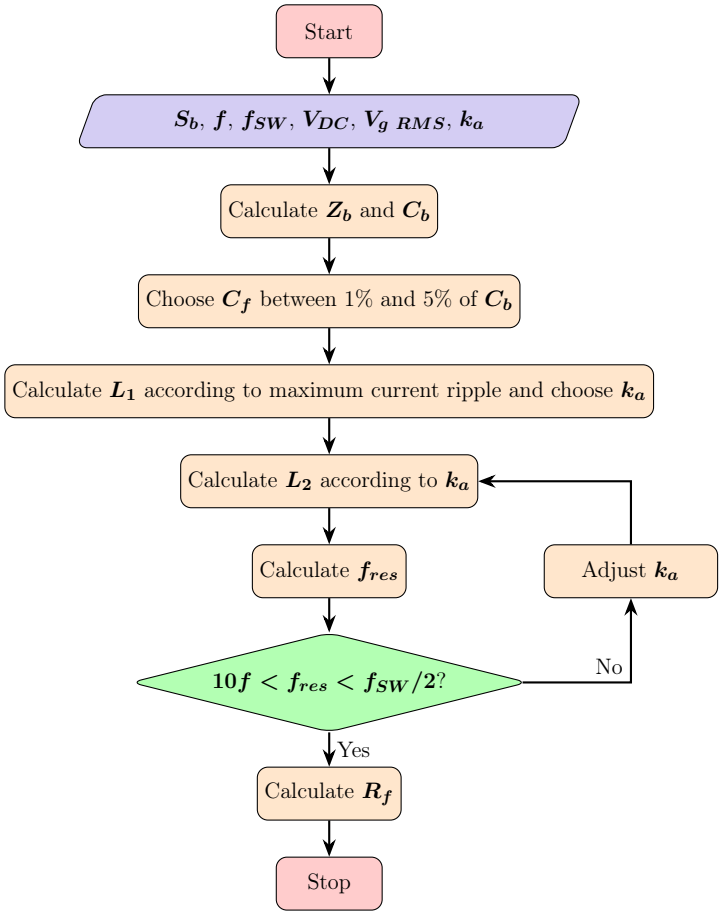
Figure 11 – Flowchart of LCL filter design strategy



Font: adapted from Reznik et al. (2014).

The value of C_f is chosen according to the percentage of power that capacitor can absorb, in other words, a percentual of S_b. Reznik et al. (2014) recommend a value between 1% and 5%. Nevertheless, a higher value of C_f can be used to compensate for the filter's inductive reactance. Mohan, Undeland and Robbins (1995) alert that a capacitance too high can increase the current ripple.

To calculate inductance L_1, Equation 2.3 is used. The equation is derived from the current ripple in a typical converter where T_{SW} is the switching period and m is

the modulation index. Since the maximum ripple occurs with $m = 0.5$, this is the value considered. The allowed current ripple is chosen to be 10% of nominal current, as in Equation 2.4, and I_{nom} is determined by Equation 2.5.

$$L_1 = \frac{2V_{DC}}{3\Delta I_{Lmax}}(1-m)mT_{SW} \overset{(m=0.5)}{=} \frac{V_{DC}}{6f_{SW}\Delta I_{L\ max}} \tag{2.3}$$

$$\Delta I_{L\ max} = 0.1 I_{nom} \tag{2.4}$$

$$I_{nom} = \frac{S_b}{V_{gRMS}} \tag{2.5}$$

Although Equation 2.3 was derived for a typical three-level inverter, Ramteke and Patil (2014) had good results using this equation to design a filter for a 5-level inverter. To determine inductance L_2, equations 2.6 and 2.7 are used. In the equation, k_a is the attenuation factor and represents the relation between the harmonic current injected in the grid and the harmonic current generated by the inverter, as in Equation 2.8. $i_g(h)$ is the harmonic current injected in the grid, and $i_{inv}(h)$ is the harmonic generated by the converter.

$$L_2 = \frac{\sqrt{\frac{1}{k_a^2}} + 1}{C_f \omega_{SW}^2} \tag{2.6}$$

$$\omega_{SW} = \pi f_{SW} \tag{2.7}$$

$$k_a = \frac{i_g(h)}{i_{inv}(h)} \tag{2.8}$$

The filter resonance frequency must satisfy the condition specified by Equation 2.9, considering f_{res} and ω_{res} as in Equation 2.10 and Equation 2.11, respectively. f_{res} must be at least a decade higher than the grid frequency to avoid voltage peaks at low frequencies and at least half the switching frequency to attenuate the harmonics produced during switching. If the condition is not met, the filter must be redesigned, as shown in the flowchart of Figure 11.

$$10f < f_{res} < 0.5 f_{SW} \tag{2.9}$$

$$f_{res} = \frac{\omega_{res}}{2\pi} \tag{2.10}$$

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \tag{2.11}$$

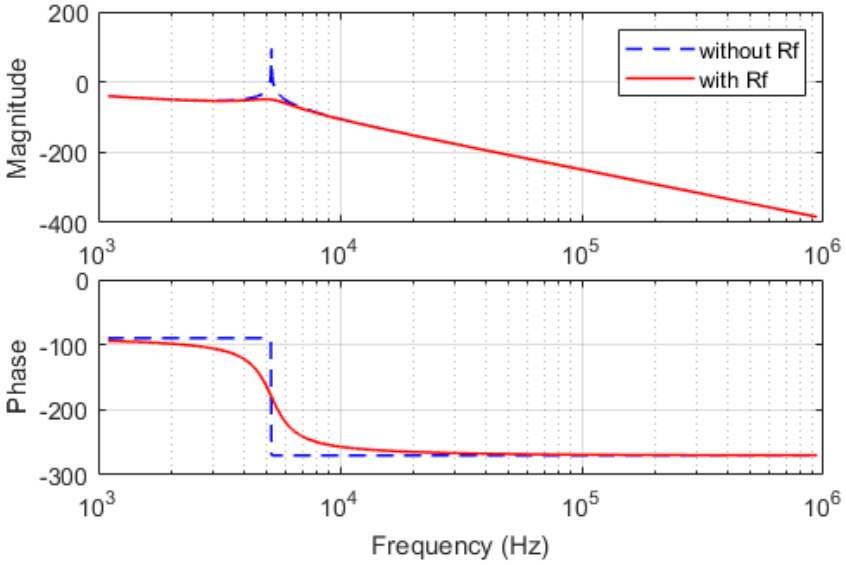
At last, the damping resistor R_f is chosen to be a third of filter impedance at resonance frequency as in Equation 2.12 (Araujo et al., 2007). The resistor's function is to attenuate the gain peak at the resonance frequency, reducing possible amplifications at f_{res}. Figure 12 shows the Bode plot of an LCL filter with and without the damping resistor. The transfer functions ($I_g(s)/V_{inv}(s)$) without and with R_f are presented in equations 2.13 and 2.14, respectively.

$$R_f = \frac{1}{3\omega_{res}C_f} \tag{2.12}$$

$$H_{LCL}(s)_{without\ Rf} = \frac{1}{L_1C_fL_2s^3 + (L_1 + L_2)s} \tag{2.13}$$

$$H_{LCL}(s)_{with\ Rf} = \frac{C_fR_f + 1}{L_1C_fL_2s^3 + C_f(L_1 + L_2)R_fs^2 + (L_1 + L_2)s} \tag{2.14}$$

Figure 12 – Bode plot of LCL filter transfer functions



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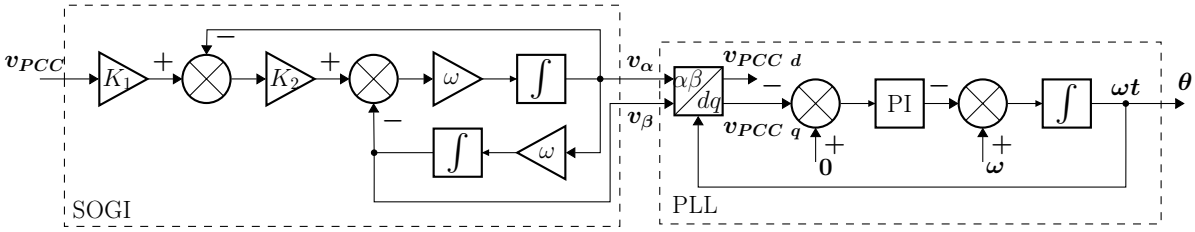
2.4 Phase-Locked Loop

Grid voltage phase, its amplitude, as well frequency, are necessary information to connect and operate the DC-AC converter. Therefore, a PLL is used to track the input voltage. This information must be accurate and fast for the inverter's control correct operation. In three-phase systems, one solution is to transform from *abc* coordinate system to synchronous *dq* coordinates and use a PI loop to lock the angle (Kaura; Blasko, 1997) and, since then, several PLL techniques are being proposed (Gawhade; Ojha, 2021). For single-phase systems, Ciobotaru, Teodorescu and Blaabjerg (2006) proposed the use of the Second-Order Generalized Integrator (SOGI) to provide orthogonal signals in phase with the grid voltage. The signal generated by a SOGI is filtered due to its structure resonance, and the SOGI-PLL is simple to implement. Figure 13 depicts the SOGI-PLL block diagram.

The gain K_1 in Figure 13 is used to normalize grid voltage and work in pu units. On the other hand, the gain K_2 is related to the SOGI response settling time, as discussed

Figure 13 – SOGI-PLL block diagram



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by Kulkarni and John (2013). The transfer functions for SOGI are in equations 2.15 and 2.16, whereas v_{PCC} is the voltage at the Point of Common Coupling (PCC) shown in Figure 3. Kulkarni and John (2013) evaluated several values for K_2 for a 50 Hz system and concluded that $K_2 = 1.57$ offered the minimum settling time of 15 ms for $G_1(s)$ and 11.6 ms for $G_2(s)$. Dash, Mishra and Mishra (2021) also tested some values for K_2, showing that smaller values offered a narrow bandwidth, enhancing the notch filter characteristic of the SOGI, at the cost of a higher settling time.

$$G_1(s) = \frac{v_\alpha}{K_1 v_{PCC}}(s) = \frac{K_2 \omega s}{s^2 + K_2 \omega s + \omega^2} \tag{2.15}$$

$$G_2(s) = \frac{v_\beta}{K_1 v_{PCC}}(s) = \frac{K_2 \omega^2}{s^2 + K_2 \omega s + \omega^2} \tag{2.16}$$

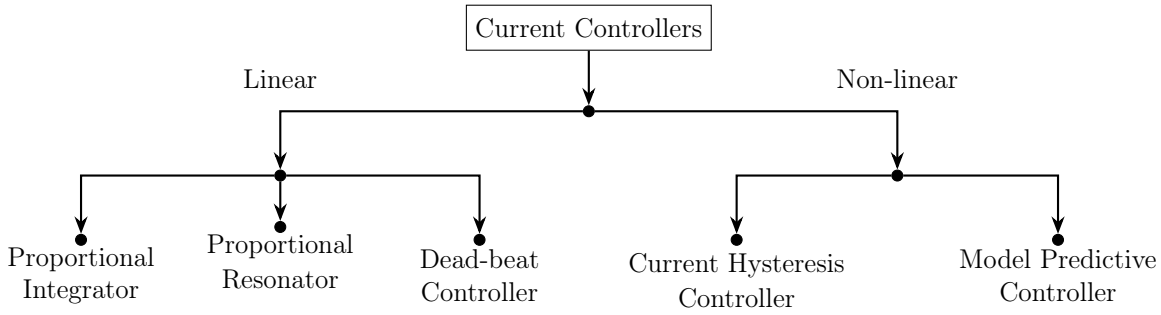
The tuning of the PLL PI controller is usually through designing the bandwidth and damping factor of the closed loop system, obtained by linearizing the PLL model (Chung, 2000). Chung (2000) presents PLL results for three PI controller designs and showed that smaller bandwidth gives slower results but more robustness to voltage harmonics while higher bandwidth results in a faster PLL, but more sensitivity to harmonic distortion.

2.5 Current Controllers

Current controllers can be classified as linear or non-linear, as shown in Figure 14. The controller implemented in this project was the Proportional Integrator Current Controller (PICC) in the synchronous reference frame. Chatterjee and Mohanty (2018) compared the control strategies of Figure 14 for a 1 kW inverter and inferred that some advantages of the PICC are good transient response and easy implementation, while disadvantages are steady-state error, strong coupling between variables, and requirement of 2 PI controllers.

Ebrahimi and Khajehoddin (2015) present a PICC consisting of PI controllers, decoupling terms, and feedforward in dq axes, as shown in Figure 15. Since the DER system under study is single-phase, a virtual β component of the current is needed. The SOGI presented in section 2.4 can be used to generate this component, and the angle

Figure 14 – Current controllers classification



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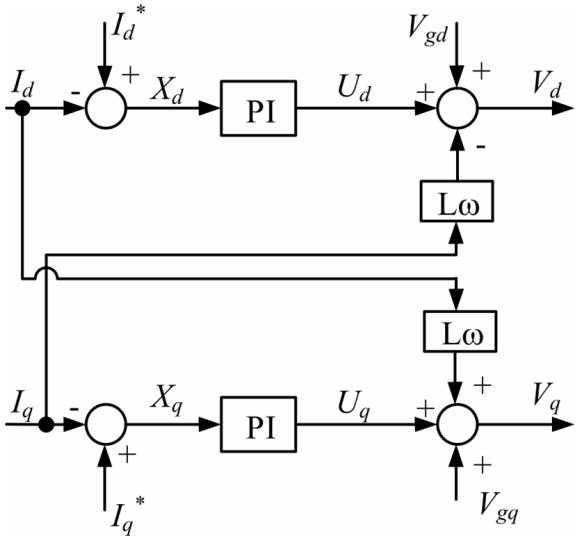
θ obtained from the PLL to apply $\alpha\beta$ to dq transform. The structure of Figure 15 is similar to the three-phase dq frame current controllers. In the figure, I_d and I_q are d and q components of the inverters current, and I_d^* and I_q^* are current references. Also, V_{gd} and V_{gq} are grid voltage d and q components of grid voltage, and V_d and V_q are d and q components of inverters voltage calculated output.

Figure 15 – Block diagram of an example of PICC



Font: adapted from Ebrahimi and Khajehoddin (2015).

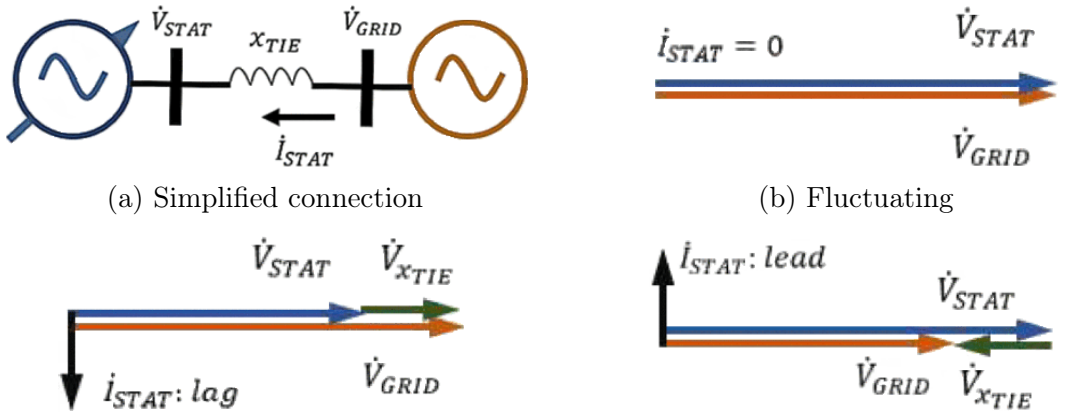
2.6 Reactive Power Compensation

Reactive power compensation has several benefits, and a STATCOM can be used for this purpose, as stated in chapter 1. To illustrate the importance of this equipment, Hingorani and Gyugyi (2000) show an example of an application at the Sullivan substation in the United States. When the STATCOM was commissioned in 1995, the substation served seven distributors and one large industrial customer and was on the edge of the transmission company service area. Consequently, the substation's power consumption

had inductive behavior during the day because of the supplied loads and a capacitive behavior during the night because of the transmission lines. The device constructed in the substation avoided the installation of a second transform bank or the construction of other lines in the area for several years.

Figure 16 shows the STATCOM's simplified connection scheme and current phasor behavior according to the relation between STATCOM voltage and grid voltage. A variable voltage source represents the compensator, while a fixed voltage source represents the grid voltage. Both sources are connected through a tie inductance shown in Figure 16a. When the voltages are equal, the current flowing is zero, and the device is said to be in idle mode, as in Figure 16b. Considering the voltages still are in phase, a current lagging the voltage appears when the compensator voltage module is smaller than the grid voltage, as in Figure 16c. On the other hand, a current leading the voltages flows if the STATCOM voltage is higher than the grid voltage, as shown in Figure 16d.

Figure 16 – Simplified connection of a STATCOM and vector diagram for different behavior



(a) Simplified connection (b) Fluctuating

(c) Inductive behavior (d) Capacitive behavior

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Equations 2.17 and 2.18 describe active and reactive power flow. In the equation, V_{GRID} and V_{STAT} are the RMS value of grid and STATCOM voltages, respectively, X_{TIE} is the reactance of the tie inductance, and δ is the angle between the equipment voltage and grid voltage. The active power flow is mainly controlled by the angle of $\dot{V}_{STAT}$, and reactive power flow mainly by adjusting the module of $\dot{V}_{STAT}$.

$$P_S = \frac{V_{GRID}V_{STAT}}{X_{TIE}} sen(\delta) \tag{2.17}$$

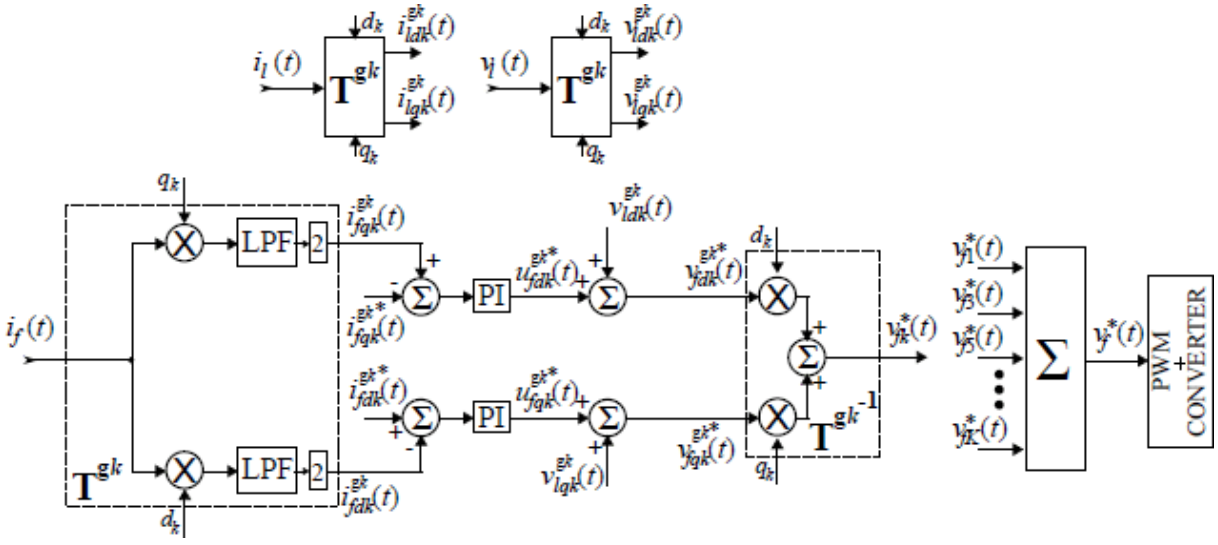
$$Q_S = \frac{V_{GRID}^2}{X_{TIE}} - \frac{V_{GRID}V_{STAT}}{X_{TIE}} cos(\delta) \tag{2.18}$$

2.7 Harmonic Compensation

A powerful tool to mitigate harmonic currents circulating in the utility grid is the use of Active Power Filters (APF) (Mattavelli, 2001). The APF operation idea is to inject the harmonic current needed by the load so that this current does not circulate through the grid. The injection of harmonic current was already explored in 1969 (Bird; Marsh; McLellan, 1969). A conventional control strategy for an APF uses the instantaneous power theory to detect and compensate for harmonics of loads (Akagi; Nabae; Atoh, 1986). However, APF's current control delay causes incorrect compensation, especially when a fully digital control implementation is used (Mattavelli, 2001).

Another solution is using a closed loop for some of the line current harmonics, with a synchronous reference frame for each of the selected harmonics (Mattavelli, 2001) (Lascu et al., 2007) (Freitas et al., 2014). For example, Figure 17 shows the strategy adopted by Freitas et al. (2014). First, grid current is measured, extracting the harmonics of interest. Then, each harmonic is transformed from the natural frame to the respective synchronous dq frame with T^{gk}, and a controller is used to derive the necessary voltage reference. This voltage reference is transformed to the natural frame with $T^{gk^{-1}}$ and summed with the others loop output. The index k is used to address each harmonic. Finally, the resulted voltage reference is sent to a PWM regulator that commands the APF. Mattavelli (2001) uses a similar strategy, but the output is a current reference sent to a current regulator.

Figure 17 – Selective harmonic compensation strategy without current controller



Font: Freitas et al. (2014).

2.8 Conclusion

This chapter provides a theoretical background with information that will base the design of the DC-AC converter control strategy. Some of this information is highlighted below:

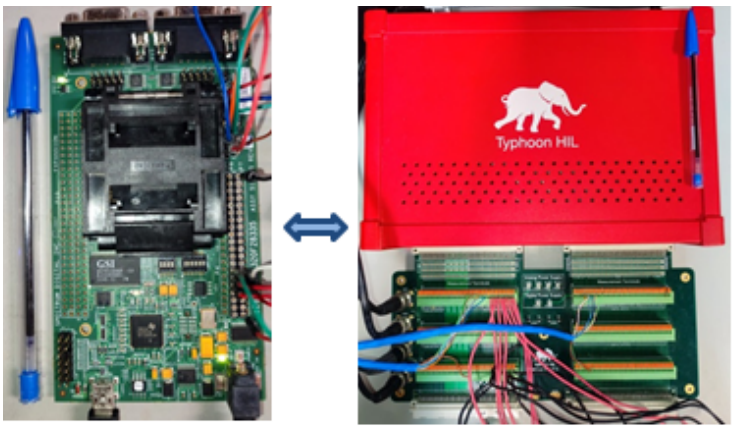
- From section 2.1, three PWM channels with two complementary outputs each are enough to drive the chosen DC-AC converter;
- To charge the battery, the converter controller should implement the charging curve of Figure 9;
- LCL filter can used to filter high order harmonics that comes from the DC-AC converter, and can be designed with the strategy proposed in section 2.3;
- A PLL can be used to synchronize the converter with the utility grid;
- Active and reactive power must be calculated, and the converter must provide lagging or leading current to regulate reactive power;
- Harmonic compensation can be implemented by extracting the frequencies to be compensated from the grid current and developing a control loop for each one;
- Measurements needed for the control realization are the grid voltage and current, the batteries' voltages and currents, and the converter current. Batteries' measurements can be sampled at a slower frequency since the monitored behavior is at a low frequency.

The next chapter will explore the methodology used to design the converter control, presenting chosen parameters, hardware, and implementation details.

3 System Description

HIL simulation was chosen to test the DC-AC converter control feasibility with a cheaper setup, and Figure 18 shows the hardware employed. A Typhoon HIL 402 emulates the power system in real-time and sends measurements through its analog outputs. An eZdspF28335 board reads those measurements, processes the information, and sends the FB-T switches command signals to Typhoon HIL. The following sections detail the methodology used to design the Typhoon HIL power system simulation and the control implemented in the eZdsp board to enhance this work's reproducibility.

Figure 18 – Test bench hardware



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3.1 Typhoon HIL 402 setup

The Typhoon HIL 402 hardware detailed description is available at Typhoon HIL (2022), and general specifications are included in Annex A. According to the manufacturer, it can model converters with switching frequencies up to 200 kHz and has 16 analog inputs and 16 outputs of 16-bit resolution, 32 digital inputs, and 32 digital outputs. Digital IO has a 20 ns update rate. Also, the simulator has four cores that the user configures according to the needs of the simulation. Core configuration 2 was chosen for this work. Figure 19 shows the system's diagram employed. Details are in Figures 20 (power converter and filter) and 21 (loads block). Two cores are necessary for this simulation, and the core coupling block was placed in the middle of the LCL filter, as shown in Figure 20b.

Figure 19 – Power system simulation diagram

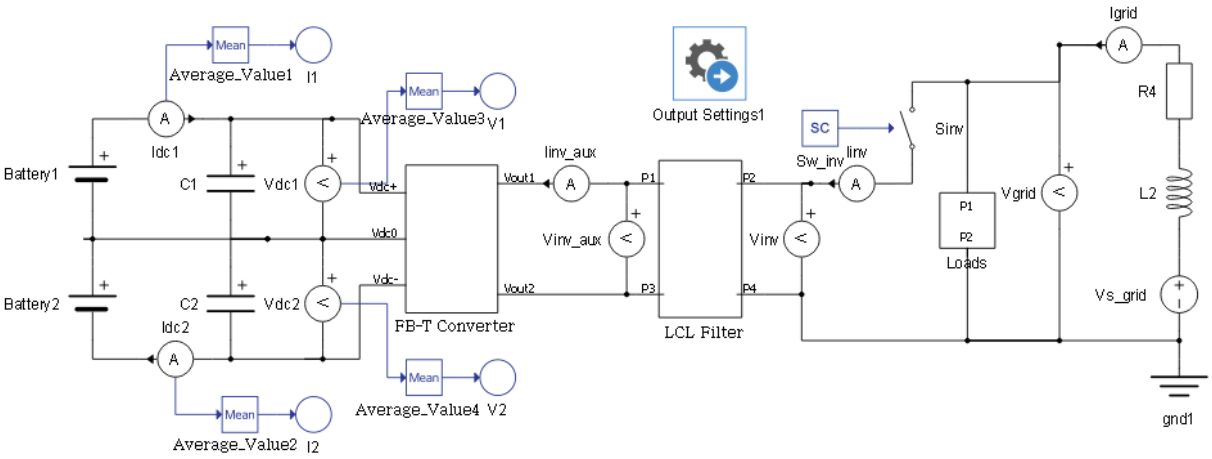

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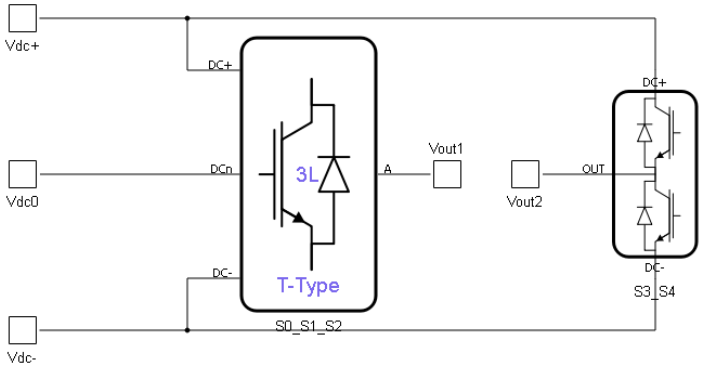
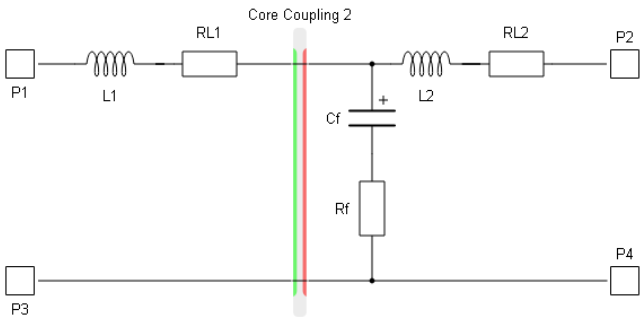
Figure 20 – Power system blocks details



(a) FB-T converter



(b) LCL filter

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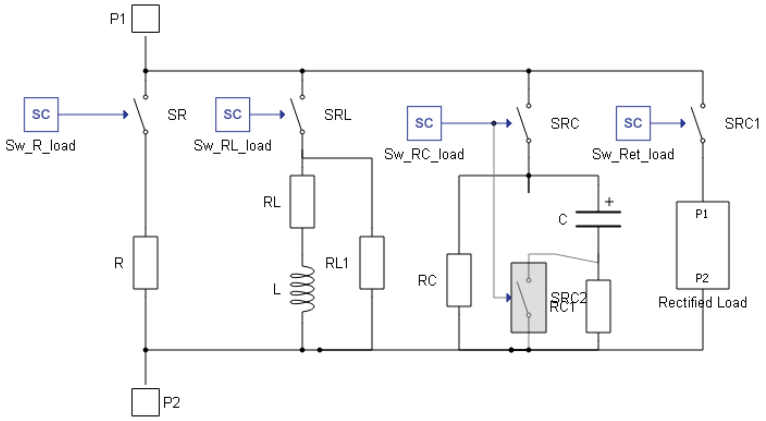
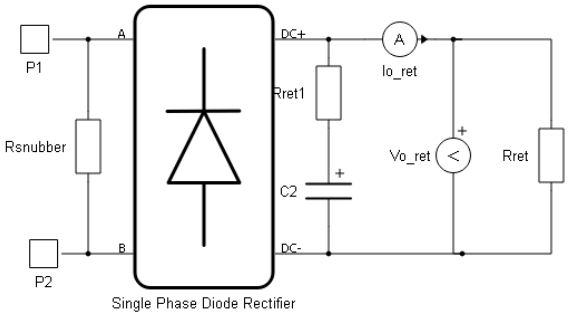
Figure 21 – Power system loads blocks



(a) Loads blocks



(b) Non-linear load (Full-wave rectifier)

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The batteries in Figure 19 are configured as a bank of eight 40 Ah 12.8 V lithium car batteries, based on the battery sold at Antigravity Batteries (2022). The specifications for the battery model used as reference is presented in Annex B. Capacitors in parallel with the battery banks are used as filters. Table 2 specifies the parameters chosen for the power system, DC-AC converter, LCL filter, and loads. The LCL filter has a calculated cut-off frequency of 6.16 kHz, and Figure 22 shows the filter's bode plot, generated with the transfer function from Equation 2.14. A low-value resistance was connected in series with the inductors of the filter to improve simulation stability. Several load types and power levels were considered. A pre-charge resistor was added to the capacitive load to avoid current peaks. This resistor is bypassed after 0.4 s from the connection of the RC load.

Figure 22 – LCL filter bode diagram

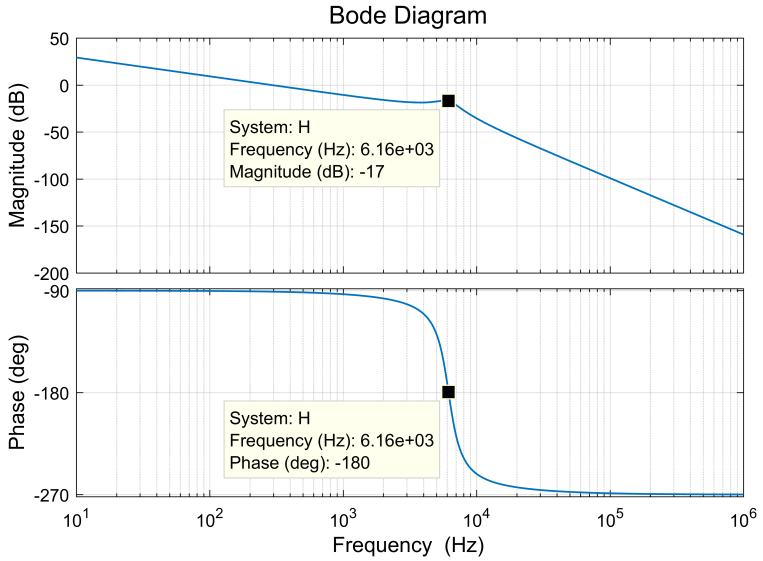

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Table 2 – Power system parameters

Description	**Symbol**	**Value**			
Power Grid					
Grid frequency	f	60 Hz			
Grid Voltage	v_{s_grid}	127 V_{RMS}			
Feeder Resistance	R_4	0.0866 Ω			
Feeder Inductance	L_2	0.159 mH			
FB-T					
Switching Frequency	f_{SW}	20.04 kHz			
Nominal Power	S_{nom}	4 kVA			
Battery banks					
Battery Nominal Voltage	$E_1,\ E_2$	102.4 V			
Filter Capacitors	$C_1,\ C_2$	1000 μF			
LCL filter					
Cut-off Frequency	f_c	6.16 kHz			
Inverter-side Inductance	L_1	0.528 mH			
Grid-side Inductance	L_2	0.021 mH			
Inductor Resistor	$RL_1,\ RL_2$	0.001 Ω			
Filter Capacitor	C	32.89 μF			
Dampening Resistor	R_f	0.261 Ω			
Loads					
Load Level	**Load Types(PF)**			**Rectifier (P_{OUT})**	
	R	**RL**	**RC**		
Light, 1 kW	1	0.71	0.71	1 kW	
Medium, 5 kW	1	0.8	0.8	5 kW	
Heavy, 10 kW	1	0.75	0.75	10 kW	

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3.2 Signal Conditioning

Typhoon HIL 402 analog IO pins leads with ±10 V, while eZdsp ADCs pins are 0-3.3 V. Additionally, Typhoon HIL digital IOs are 0 or 5 V, and eZdsp are 0 or 3.3 V. To avoid damage to the microcontroller, two signal conditioning PCBs were made, one consisting of the RC divider circuit of Figure 23 to conditioning analog signals, and the other using an SN7407N IC with pull-up and pull-down resistors to conditioning digital signals. Figures 24a and 24b show the Analog and Digital PCB, respectively.

Figure 23 – Analog signal conditioning circuit

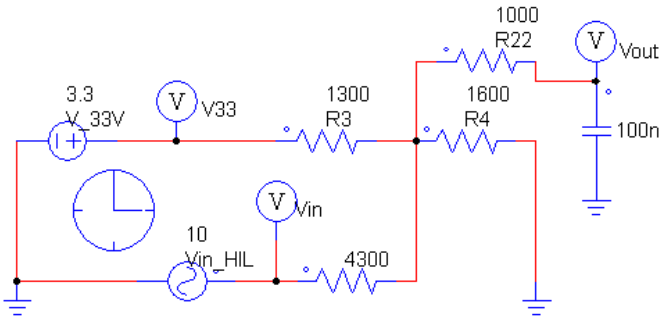

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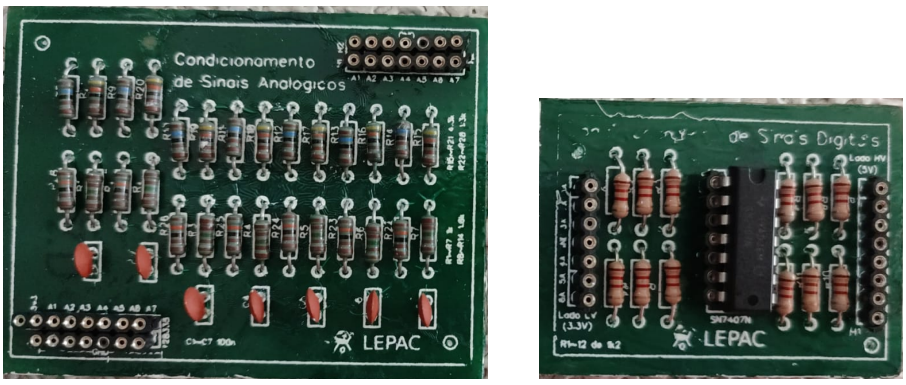
Figure 24 – Signal conditioning PCB



(a) Analog signals PCB (b) Digital Signals PCB

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3.3 eZdsp F28335 setup

The eZdsp F28335 is a development board produced by Spectrum Digital, and the board is equipped with a TMS320F28335 digital signal controller. The Micro-Controller Unit (MCU) runs at a clock of 150 MHz and can perform 150 mega instructions per second. It has up to 18 PWM outputs and 16 12-bit ADC channels. All ADC channels are accessed at the same time, but its lecture by the MCU is asynchronous. About the

18 PWM outputs, 12 channels are generated by 6 EPWM (enhanced PWM) modules that incorporate hardware support to dead band generation. More information about the development board and the F28335 MCU can be consulted at Spectrum digital (2007) and Texas instruments (2007). The MCU's features and functional block diagram is presented in Annex C.

To program the microcontroller, the software Code Composer Studio was used. The software is designed by Texas Instruments, the same manufacturer of the MCU. It has debugging tools and allows to access variables in the DSP's memory to facilitate the design. The newest version of Code Composer compatible with the eZdsp is version 8, and therefore it is the version used in this project.

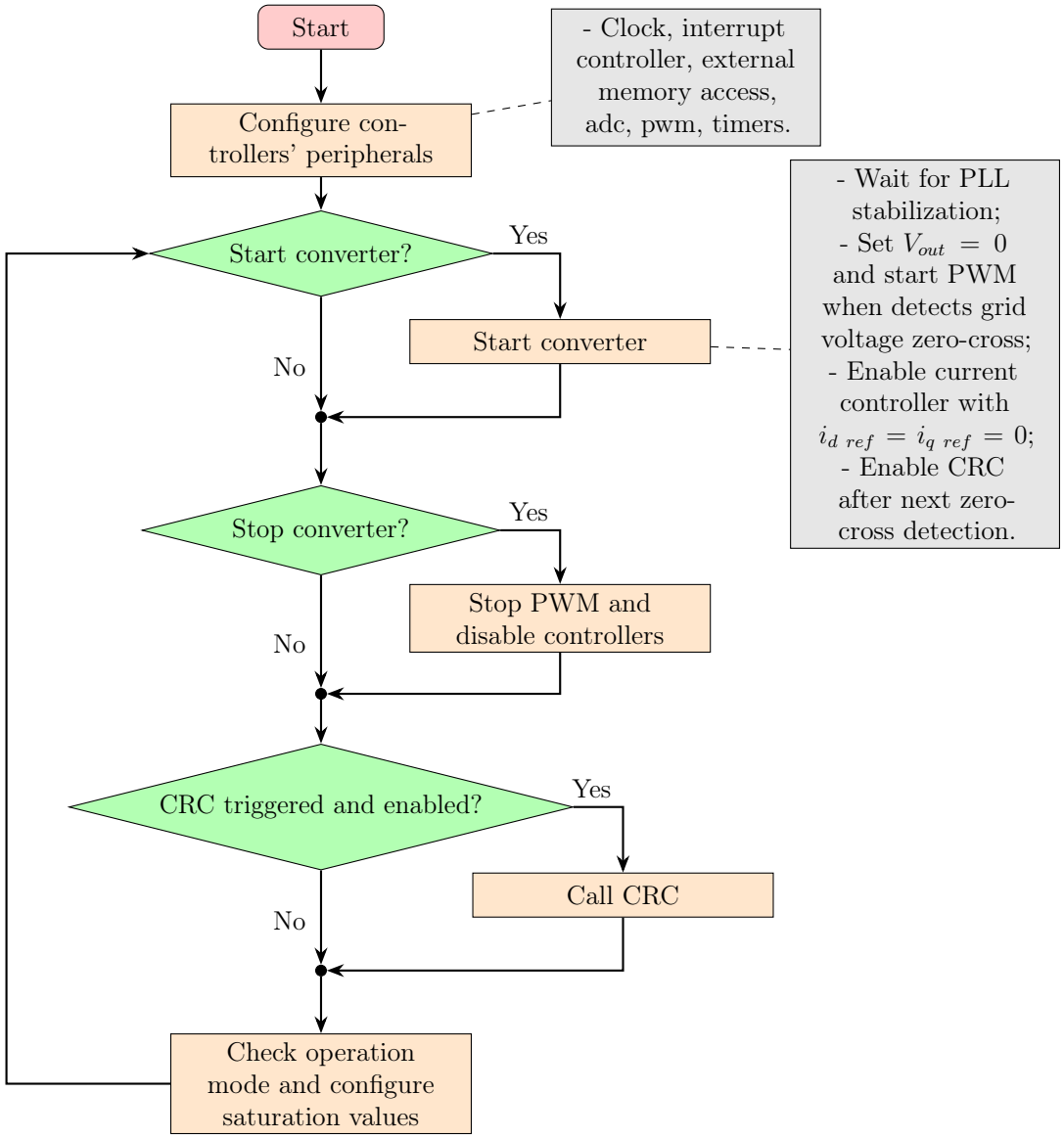
The MCU is set to work at maximum clock speed (150 MHz), and only the peripherals that are used have their clock enabled, specifically, the ADC unit, EPWM modules 1, 2, 3, CPU timers 0, 1, 2, and external memory block. The sections below will explain how the controller logic is implemented.

3.3.1 Main routine and operation modes

The main routine of the converter has a system setup part, executed once, and a looping part. In the loop, the program is responsible for starting or stopping the converter's operation, calling the Converter's Reference Control (CRC) routine when triggered, checking the device's operation mode, and setting the saturation values according to the functions activated. Figure 25 presents a flowchart of the main routine logic.

Four operation modes and two security modes are configured in the controller: battery charge, STATCOM, harmonic current compensation, power export, force charge, and force discharge. The security modes activate to charge and discharge the batteries when their voltages reach risky values. And operation modes change the maximum values $i_{d\ max}$ and $i_{q\ max}$ so that the converter focuses on the chosen function. Nevertheless, it does not mean the converter can't operate with other functions activated. For instance, if in battery charge mode, it can also function as STATCOM and with harmonic compensation if those functions are enabled. But, most of its power capacity is dedicated to charging the battery, following the charging curve in Figure 9. As other example, when operating in STATCOM mode, the device can charge the battery and compensate for harmonics if those functions are enabled. However, most of the power processing capacity is reserved for reactive power. Therefore the battery would charge slowly, using the constant voltage controller with a small maximum current. More details of each mode and given limits are described in sections 3.3.1.1, 3.3.1.2, 3.3.1.3, 3.3.1.4, and 3.3.1.5.

Figure 25 – Flowchart of converter's main routine



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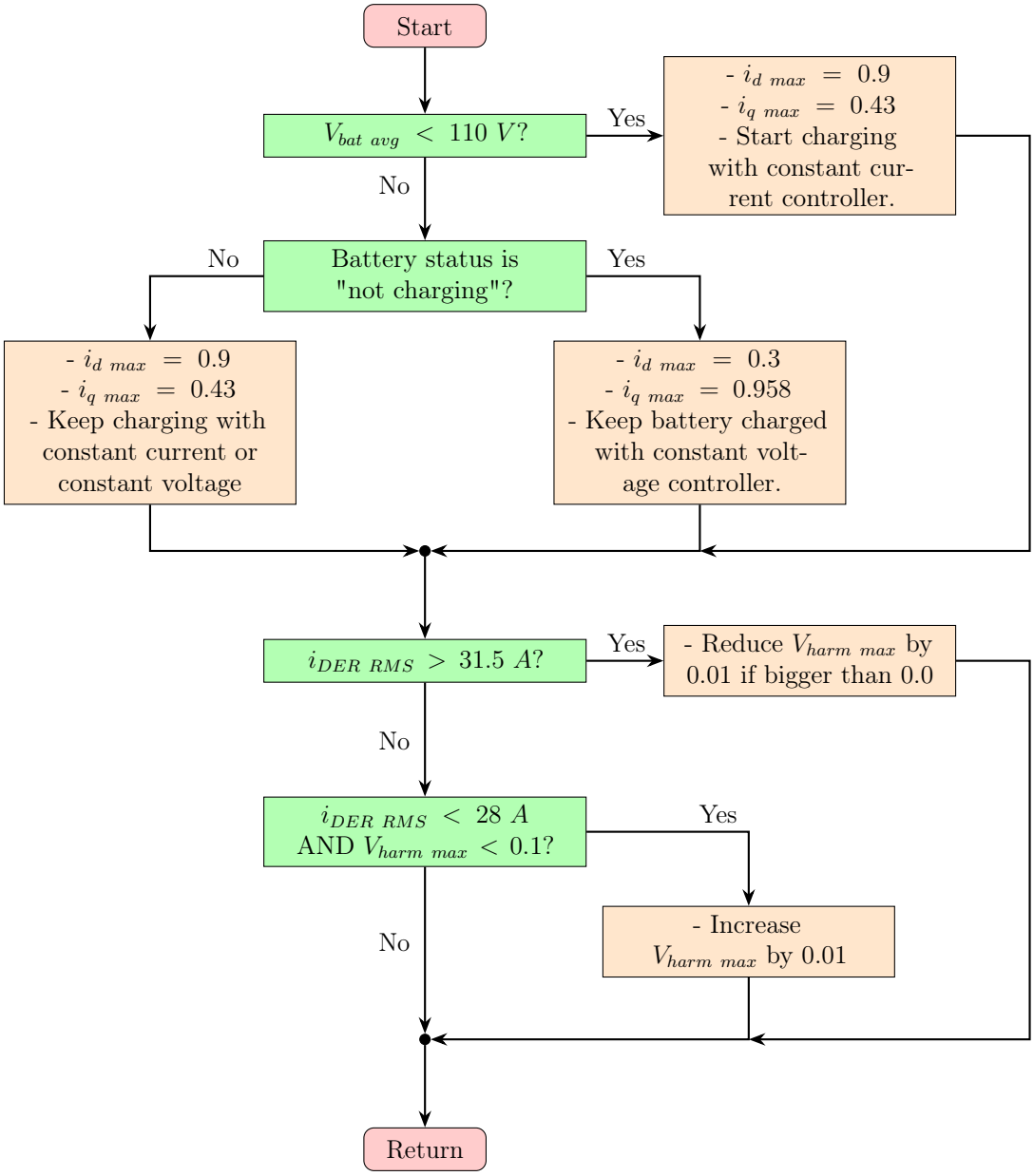
3.3.1.1 Battery charge mode

The flowchart in Figure 26 describes the setup process and limits chosen in this mode. First, it verifies if the average voltage of the batteries is lower than 110 V. If yes, it starts the charging process with the constant current control and defines a high value for $i_{d\ max}$. If the voltage is above 110V, then it verifies if the battery is still charging. If yes, it keeps $i_{d\ max}$ high. However, if the batteries are fully charged, the current is expected to reduce, so it defines a lower value for $i_{d\ max}$ and a higher value for $i_{q\ max}$. The current limits $i_{d\ max}$ and $i_{q\ max}$ satisfy $\sqrt{i_{d\ max}^2 + i_{q\ max}^2} \leq 1.0$ so that the inverter's reference current keeps below the rated value.

The limit for harmonic compensation $v_{harm\ max}$ reduces slowly if the converters' RMS current ($i_{DER\ RMS}$) is above 31.5A. If $i_{DER\ RMS}$ reduces below 28A, the limit for

harmonic compensation increases slowly again, up to $V_{harm\ max} = 0.1$.

Figure 26 – Flowchart of battery charge mode setup



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3.3.1.2 STATCOM mode

The configuration for the STATCOM mode first verifies if the batteries' voltage allows for a safe operation. If the average voltage of the batteries is between 95 V and 115.2 V, then the routine defines a high value for $i_{q\ max}$. If the voltage is between 93 V and 95 V, the device reserves a small portion of the current capacity for absorbing active power from the grid and tries to charge the batteries. If the voltage falls below 93 V, the converter is forced to charge the battery and disable all other functions, if activated. On the other hand, if the voltage is between 115.2 and 118 V, the routine reserves capacity for exporting

active power and tries to discharge the batteries to their end charge voltage. If the voltage still increases, the converter shuts down STATCOM and harmonic compensation functions and switches to the force discharge mode. A small hysteresis was added to prevent the oscillations near the voltage limits. If the voltage is between 95 V and 115.2 V, the routine verifies if the converter was forced to charge or discharge in a previous loop run. If yes, a small current capacity is reserved for $i_{d\ max}$. Then, the routine verifies if the force charge or discharge can be disable. The forced charge is disabled when the voltage is between 97 V and 100 V and the forced discharge is disabled when between 109 V and 112 V. In this routine, the harmonic compensation is limited in the same way of the battery charge mode, reducing the compensation limit if $i_{DER\ RMS}$ is above 31.5 A. Figure 27 shows the flowchart for the STATCOM mode configuration.

Similarly as in the battery charge mode, the current limits $i_{d\ max}$ and $i_{q\ max}$ satisfy $\sqrt{i_{d\ max}^2 + i_{q\ max}^2} \leq 1.0$ to keep the inverter's reference current below the rated value.

3.3.1.3 Harmonic current compensation mode

In the harmonic current compensation mode, both $i_{d\ max}$ and $i_{q\ max}$ are reduced, and $V_{harm\ max}$ is bigger to focus on the harmonic compensation. This mode verifies if the battery voltage is at a safe operation level in the same way that was described in the STATCOM mode. Figure 28 shows the flowchart of the harmonic compensation mode setup routine.

3.3.1.4 Power export mode

The power export mode focuses on exporting active power from the batteries to the grid. The routine reserves a small portion of power capacity for reactive power if the batteries' average voltage is below 115.2 V. But if the voltage is higher, the controller dedicates the total capacity to active power control and deactivates STATCOM and harmonic compensation functions. This mode uses the battery constant voltage control loop with a voltage reference of 95 V. If the voltage falls below 93 V, the converter automatically starts charging the batteries but does not change the operation mode. When the batteries are fully charged, the converter starts exporting power again. Figure 29 depicts the flowchart of the power export mode setup.

Figure 27 – Flowchart of STATCOM setup

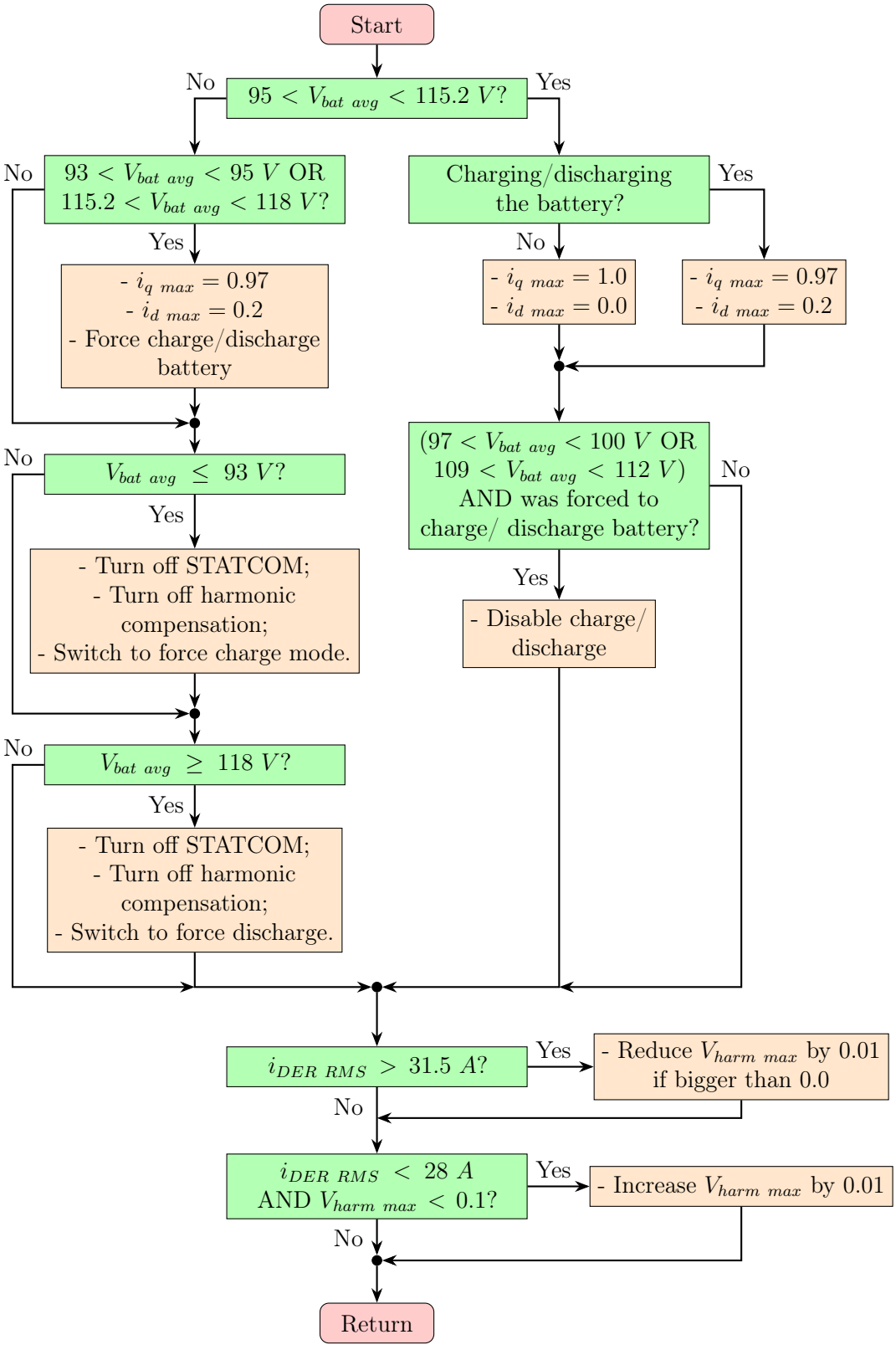

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Figure 28 – Flowchart of harmonic compensation setup

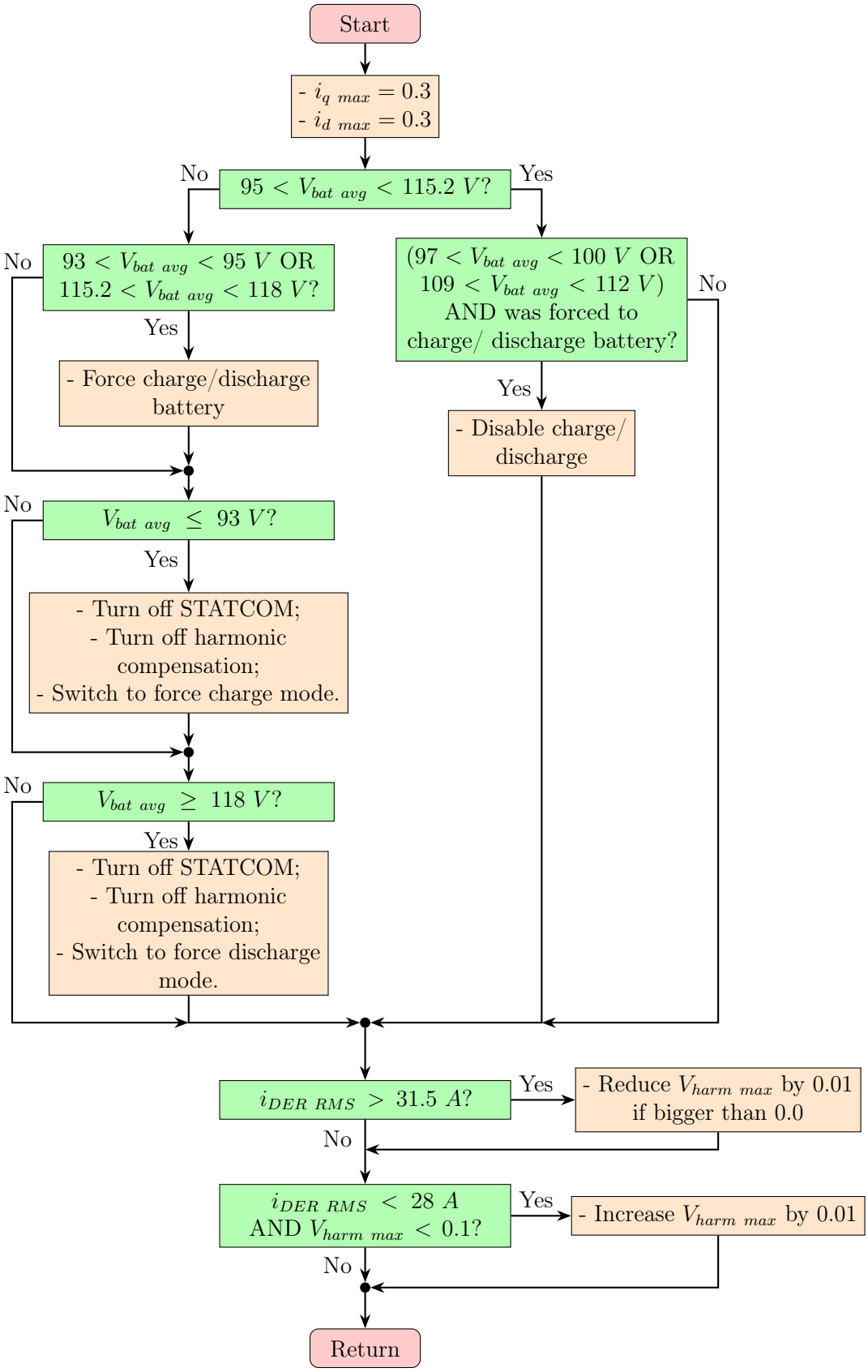

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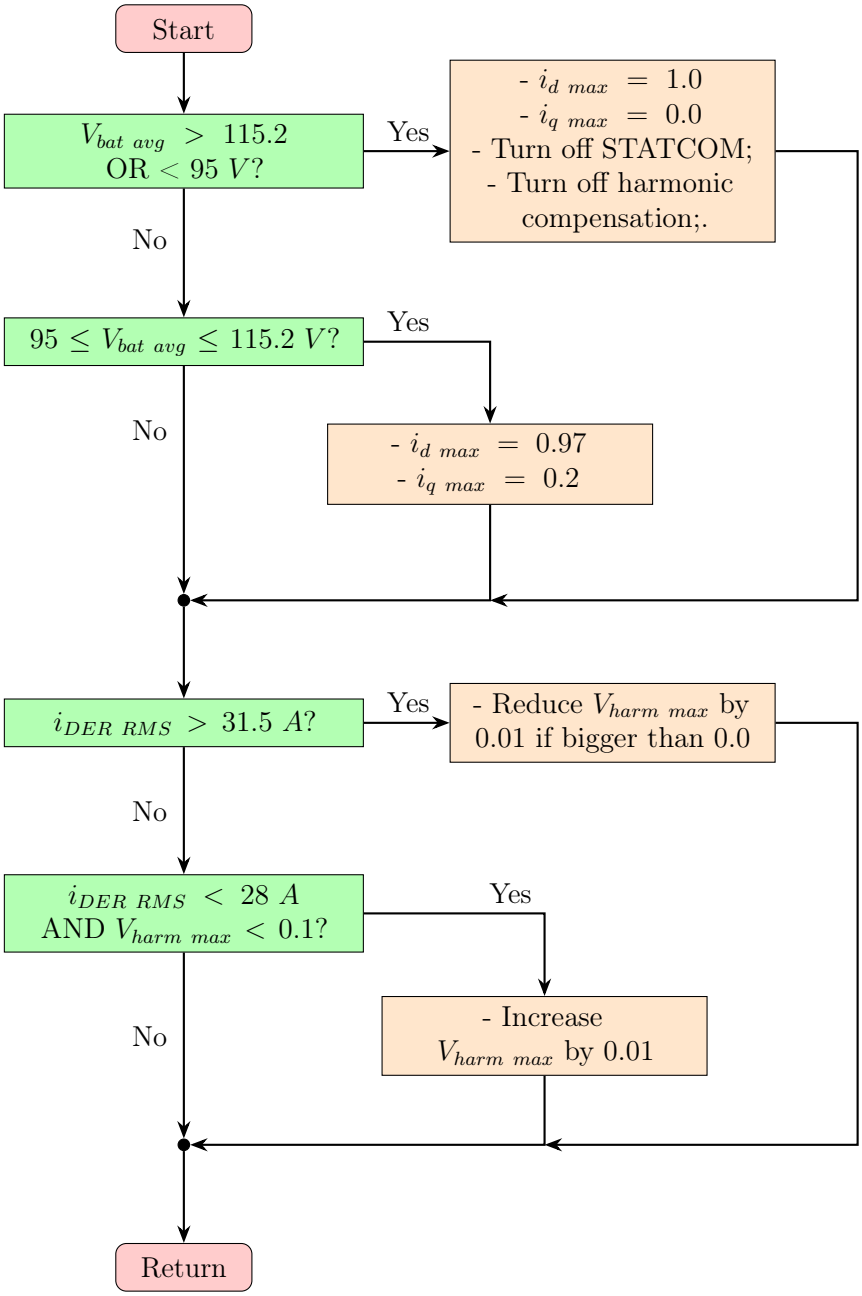
Figure 29 – Flowchart of power export mode configuration



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3.3.1.5 Force charge/discharge mode

These two modes operate when the converter functions in STATCOM or harmonic compensation mode and the batteries' voltage reaches an unsafe value. If the voltage is too high ($\geq$118V), the force discharge mode is applied, and if the voltage is too low, the force charge mode is chosen ($\leq$93V).

The configurations of these modes are very straightforward. Both deactivates STATCOM and harmonic compensation functions and sets $i_{d\ max} = 1.0$ and $i_{q\ max} = 0.0$. The difference is that in force discharge mode, the converter switches back to the previous operation mode when the voltage of the batteries is less than 112V. Meanwhile, the force charge mode switches back to the previous operation mode when the voltage of the batteries is greater than 112V.

3.3.2 Peripherals Setup

The sections below explain how the MCU's peripherals were configured.

3.3.2.1 Timers and interrupts

The three CPU timers available at the MCU are used. Timer 0 triggers an interrupt that calls the Converter's References Control (CRC) routine once every grid cycle (16.67 ms). CRC will be explained later in subsection 3.3.5.

Timer 1 triggers grid measurement routines at 10.8 kHz (every 92.59 μs). At last, Timer 2 starts battery measurement routines at 960 Hz (every 520.83 μs). Both grid and battery measurement routines will be explained in subsubsection 3.3.2.3.

The timers were selected based on their interrupt priority. The priority table of the interrupts used in this project is listed in Table 3. PWM interrupt has the highest priority due to switches control sensibility, followed by the ADC conversion interrupts, the measurements interrupts, and CRC.

3.3.2.2 PWM module

Each PWM module is provided with two channels (A and B) that can be configured to operate independently or synchronized with each other. Three of the available PWM modules are used, EPWM1, EPWM2, and EPWM3. The modules are configured to use a triangular carrier in symmetrical up-down count mode. A Rising Edge Delay (RED) and a Falling Edge Delay (FED) are configured to allow switches to finish turning off (dead time). Both delays are of 1 μs (lower time step allowed in the used HIL simulations). Figure 30 shows an example of a carrier and its relation to PWM outputs. The difference between Figure 30 and the waves used here is that in Figure 30, RED is configured in channel A and FED in channel B, while in this project, RED and FED were configured in

Table 3 – Interrupts priority table

Priority	**Block responsible**	**Functions Summary**
0 (highest)	PWM cycle	Update PWM duty cycle
1	ADC EOC	Analog to digital end of conversion
2	Timer 1	Measures and processes grid variables and calls current control routines that define voltage reference
3	Timer 2	Measures battery variables and calls harmonic compensation routines
4	Timer 0	Sets CRC flag to trigger current references update

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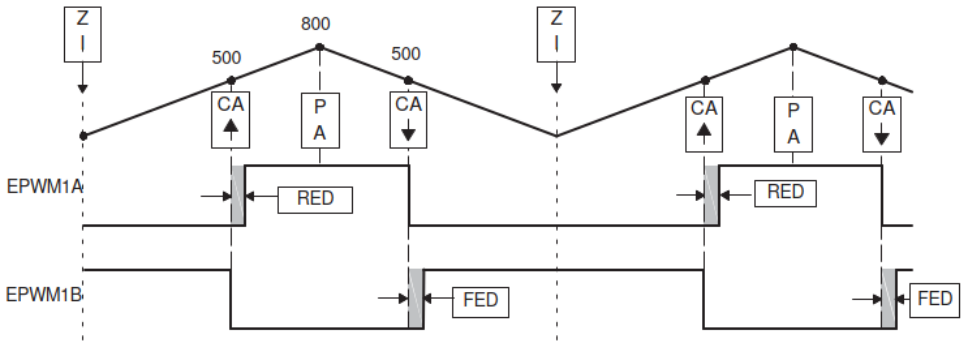
both channels for each module, so the waveform keeps symmetrical. In other words, one channel turn off a bit early and its complementary turn on a bit later. All PWM channels are synchronized with EPWM1, sharing the same triangular carrier of 20.04 kHz.

Figure 30 – PWM waveform example



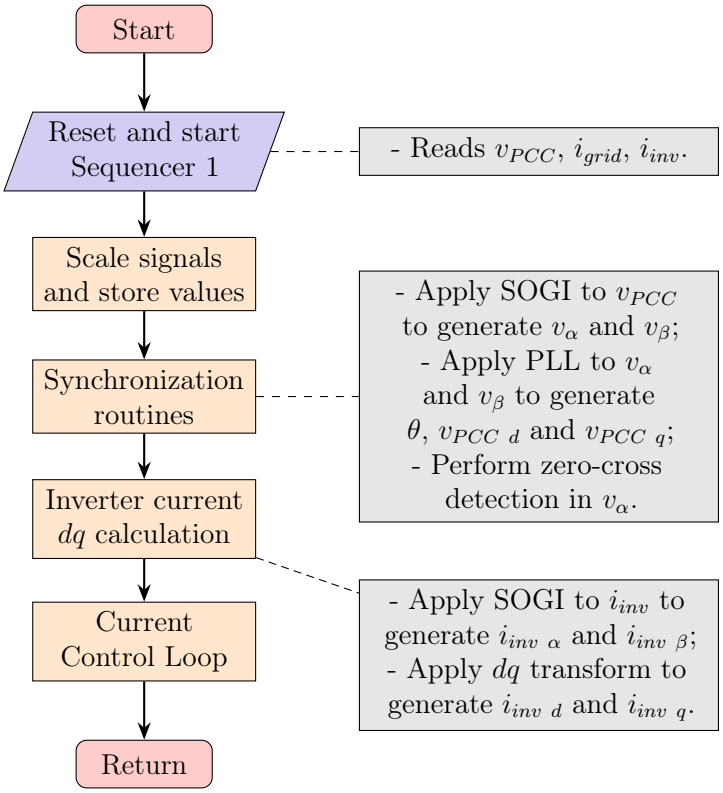
Font: Texas instruments (2020).

At the end of every cycle, the EPWM1 triggers an interrupt that calls the routines to calculate the duty cycle for each PWM module, using the modulation strategy discussed in subsection 2.1.1 and the voltage reference calculated by the current controller that is detailed in subsection 3.3.3. The duty cycles are stored in shadow registers and updated simultaneously at the top and the bottom of the PWM carrier wave.

3.3.2.3 Analog to Digital Conversion

The ADC module is also set to its maximum clock speed (25 MHz), and two sequencers were configured. Sequencer 1 measures grid voltage, grid current, and inverter current, while sequencer 2 measures the voltages and currents of the two battery banks. Two functions are responsible for starting the ADC's sequencers. The first is called grid measurements, and the second is battery measurements. The flowchart of Figure 31 summarizes the grid measurements routine, triggered every 10.8 kHz by Timer 1.

Figure 31 – Grid measurements routine



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The routine starts with the ADC readings, and each measurement is an integer value between 0 and 4095 (12 bits resolution). Therefore, each reading needs to be scaled and mapped into the real value according to the scale configured in Typhoon HIL. As an example, for v_{PCC}, 1 V in the Typhoon HIL analog output channel corresponds to 25 V in the simulation. Since HIL outputs ±10 V, this leads to 500 V mapped into 4096 values. Therefore, 1 integer in the ADC reading, corresponds to about 0.122 V. So to obtain the real value of the grid voltage, the ADC reading is subtracted by 2047 and multiplied by 0.122. Same logic applies to other measurements, but different scales were configured. Table 4 shows the scale output by HIL and corresponded resolution.

Table 4 – Scaling factors per variable

Variable	**Scale in HIL**	**Conversion resolution**
v_{PCC}	25 V/V	0.122 V
i_{grid}	15 A/V	0.073 A
i_{inv}	15 A/V	0.073 A
$v_{bat\ 1}$	15 V/V	0.073 V
$v_{bat\ 2}$	15 V/V	0.073 V
$i_{bat\ 1}$	10 A/V	0.049 A
$i_{bat\ 2}$	10 A/V	0.049 A

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SOGI and PLL block mentioned in the flowchart is the loop shown in Figure 13. The gains used are defined in Table 5, and SOGI's Bode plots of functions G_1 and G_2 (equations 2.15 and 2.16) are in Figure 32. The current controller routine is detailed in subsection 3.3.3.

Table 5 – SOGI and PLL gains

Description	Symbol	Value
SOGI		
Normalization gain	K_1	180
Loop gain	K_2	1.4
Frequency	ω	376.99 rad/s
PLL		
Proportional gain of PI controller	K_P	3769.91
Integral gain of PI controller	K_I	1316.0

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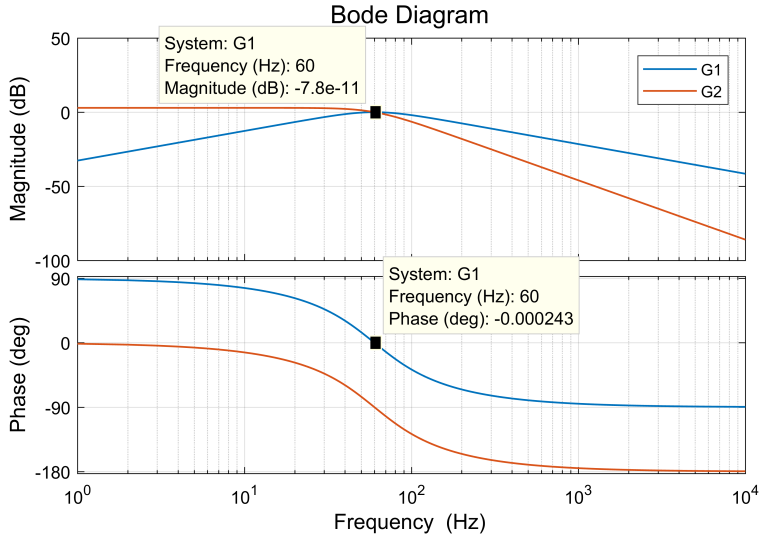
Figure 32 – SOGI's functions bode plots



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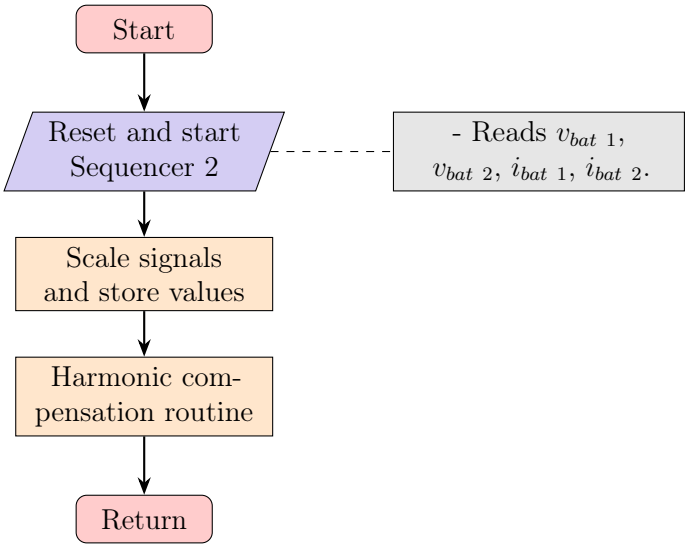
The flowchart of Figure 33 describes the battery measurements routine, triggered every 960Hz by Timer 2. As shown in the flowchart, this routine also calls for the harmonic filter routine. It would be better to update the harmonic compensation voltage at a higher frequency, such as 10.8kHz, inside the grid measurements routine. However, this was not possible due to limitations in the hardware processing power. Subsection 3.3.4 details the harmonic compensation routine.

Figure 33 – Battery measurements and harmonic compensation routine



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3.3.3 Current Controller

The current control loop was designed with one loop for the d axis, one for the q axis, feed-forward terms, and decoupling terms, similar to the loop designed by Ebrahimi and Khajehoddin (2015). In the modeling of a current controller for a Voltage Source Converter (VSC), a coupled term $L\omega i_d$ appear in i_q loop and $L\omega i_q$ in i_d loop. Therefore decoupling terms are necessary to reach two decoupled first-order linear systems (Yazdani; Iravani, 2010). Figure 34 shows the block diagram for the current controller, and the differences between Figures 34 and 15 are due to the signal conventions adopted. Table 6 shows the parameters chosen. The battery charge controller sets the current reference $i_{d\ ref}$, while the reactive power controller sets $i_{q\ ref}$. The maximum value for each reference changes according to the equipment operation mode, as detailed in subsection 3.3.5. At the end of the loop, the result is summed with the harmonic compensation signal v_{harm} to produce the voltage reference sent to the PWM.

Table 6 – Current control loop gains

Description	**Symbol**	**Value**
Proportional gain of d-loop	K_{Pd}	0.01
Integral gain of d-loop	K_{Id}	1.8
Proportional gain of q-loop	K_{Pq}	0.025
Integral gain of q-loop	K_{Iq}	2.3
Feed-forward gain	K	0.01563

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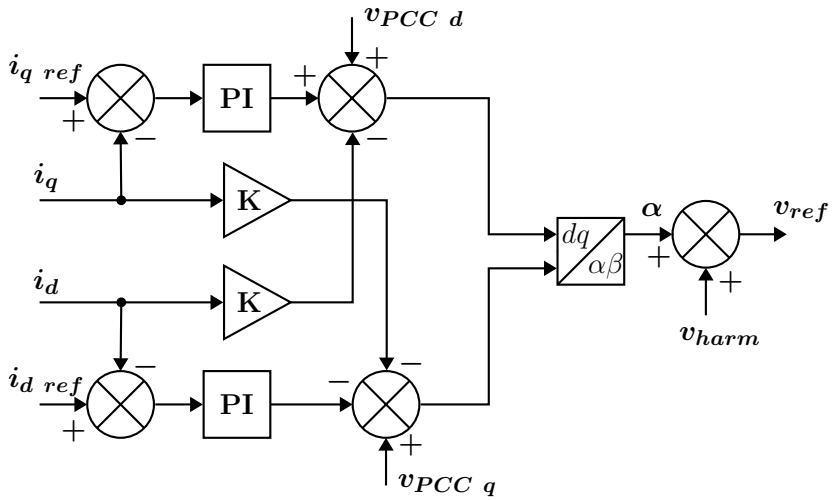
Figure 34 – Current control loop



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3.3.4 Harmonic Current Compensation

The harmonic current compensation routine uses a modified version of the strategy shown in Figure 17. The modifications consist of using a SOGI to generate the orthogonal components and signal changes due to the adopted convention. Figure 35 shows the block diagram of the harmonic compensation routine. The signal θ is produced by the PLL in the grid measurements routine, and θ is multiplied by n to select the n^{th}-harmonic. In this project, only the third, the fifth, and the seventh harmonics are compensated. There are two reasons to do so: these harmonics are usually the most important in single-phase grid, and the routine execution rate does not enable the compensation of higher order harmonics. Increasing the execution rate would also require more processing speed. The SOGI gains and the PI controllers' gains are the same for all harmonics and axis, as described in Table 7. Only the frequency of SOGI changes along with the harmonic order. The gains were obtained based on experiments results.

Table 7 – Harmonic compensation gains

Description	**Symbol**	**Value**
SOGI normalization gain	K_1	1/44.54
SOGI loop gain	K_2	0.05
3^{rd} harmonic frequency	ω_3	1130.973 rad/s
5^{th} harmonic frequency	ω_5	1884.956 rad/s
7^{th} harmonic frequency	ω_7	2638.938 rad/s
Proportional gain of controllers	K_P	0.17
Integral gain of controllers	K_I	3.8

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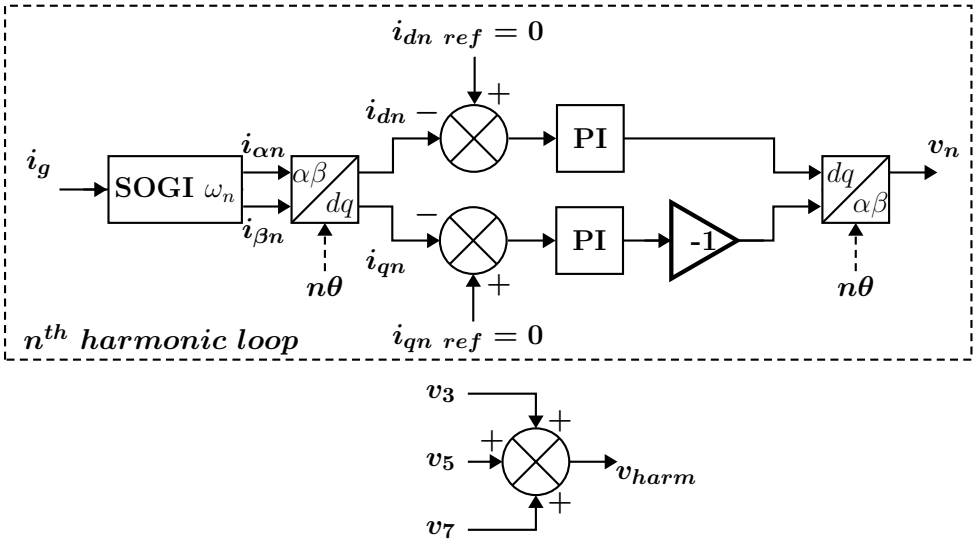
Figure 35 – Harmonic compensation block diagram



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3.3.5 Converter's Reference Control

The CRC routine is triggered every grid cycle (60 Hz) and is responsible for defining the control references for the inverter's current controller. The flowchart in Figure 36 summarizes the calculations performed in the routine. The power calculation method, battery charge controller, and reactive power controller are detailed in subsections 3.3.5.1, 3.3.5.2, and 3.3.5.3, respectively.

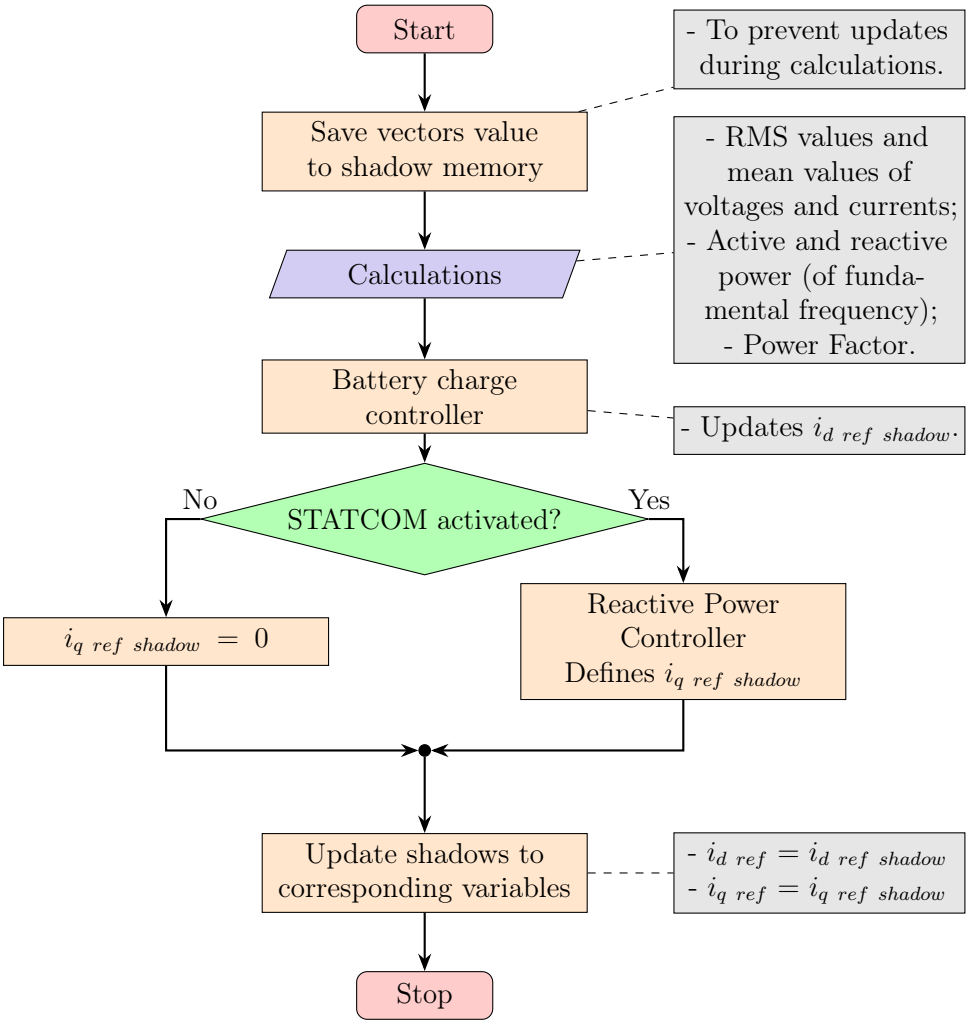
3.3.5.1 Power Calculation

Real and imaginary parts of the phasors are extracted through a Discrete-time Fourier Transform to calculate active and reactive power at the fundamental frequency, using measurements collected over a cycle. Equations 3.1 and 3.2 show how the real and imaginary parts are calculated. In the equations, n is the sample index, k is the k^{th} harmonic, x is the signal vector (voltage or current), and N is the total number of samples. Here, only the fundamental frequency is calculated, so $k = 1$, and because of the measurements sample rate of 10.8 kHz, a cycle consists of $N = 180$ samples.

$$Re\{X[k]\} = \frac{2}{N}\sum_{n=0}^{N-1} x[n]sin(2\pi kn/N) \tag{3.1}$$

$$Im\{X[k]\} = \frac{2}{N}\sum_{n=0}^{N-1} x[n]cos(2\pi kn/N) \tag{3.2}$$

Figure 36 – Flowchart for Converter's Reference Control routine



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After calculating real and imaginary parts, the module and phase of voltage and current at fundamental frequency are calculated through equations 3.3 and 3.4. Finally, active and reactive power are calculated using equations 3.5 and 3.6.

$$|X[k]| = \sqrt{Re\{X[k]\}^2 + Im\{X[k]\}^2} \tag{3.3}$$

$$\theta_{X[k]} = tan^{-1}(Im\{X[k]\}/Re\{X[k]\}) \tag{3.4}$$

$$P_{60Hz} = \frac{|V_{PCC\ 60Hz}| \cdot |I_{grid\ 60Hz}|}{2} cos\left(\theta_{V_{PCC\ 60Hz}} - \theta_{I_{grid\ 60Hz}}\right) \tag{3.5}$$

$$Q_{60Hz} = \frac{|V_{PCC\ 60Hz}| \cdot |I_{grid\ 60Hz}|}{2} sin\left(\theta_{V_{PCC\ 60Hz}} - \theta_{I_{grid\ 60Hz}}\right) \tag{3.6}$$

3.3.5.2 Battery charge controller

The battery charge controller consists of two control loops chosen according to the charging stage. The first is a current control loop that calculates $i_{d\ ref}$ during the constant current phase of the battery charger. On the other hand, the second loop is a voltage

controller that chooses $i_{d\ ref}$ during the constant voltage stage and for maintaining the battery voltage during other operation modes, absorbing power to compensate for losses. Also, the voltage loop calculates $i_{d\ ref}$ when the converter exports active power.

Figure 37a shows the current control loop, and Figure 37b shows the voltage control loop. I_{mean} is the mean value of both batteries' currents, collected at 960 Hz over a grid cycle (16.67 ms) and divided by 20 for normalization. Similarly, V_{mean} is the mean value of both batteries' voltages, divided by 115.2 for normalization. The gains defined in the loops and the references used are described in Table 8. The current control loop is selected when the batteries are at low voltage and need to charge fast. When V_{mean} reaches 115.2 V, the voltage control loop operates, and the current slowly diminishes until 10% of battery capacity, when the charging process ends. The converters' main routine defines a saturation value for $i_{d\ ref}$. The value of 115.2 V corresponds to 3.6 V per cell of the battery and is 0.05 V below of the maximum value recommended by (Antigravity Batteries, 2022). In Annex B, the maximum charge voltage of 14.6 V, defined in the battery pack specifications, corresponds to 3.65 V per cell.

Figure 37 – Battery charger control loops

(a) Current control loop (b) Voltage control loop

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Table 8 – Battery charge controllers' gains

Description	**Symbol**	**Value**
Batteries' Nominal Capacity	C	40 Ah
Current control loop		
Proportional gain	K_P	0.1
Integral gain	K_I	0.2
Charging current	I_{charge}	$0.4 \cdot C = 16$ A
Current reference	$I_{mean\ ref}$	0.8 pu
Voltage control loop		
Proportional gain	K_P	5
Integral gain	K_I	25
End charge voltage	V_{charge}	$3.6\ V/cell = 115.2$ V
Voltage reference	$V_{mean\ ref}$	1.0 pu

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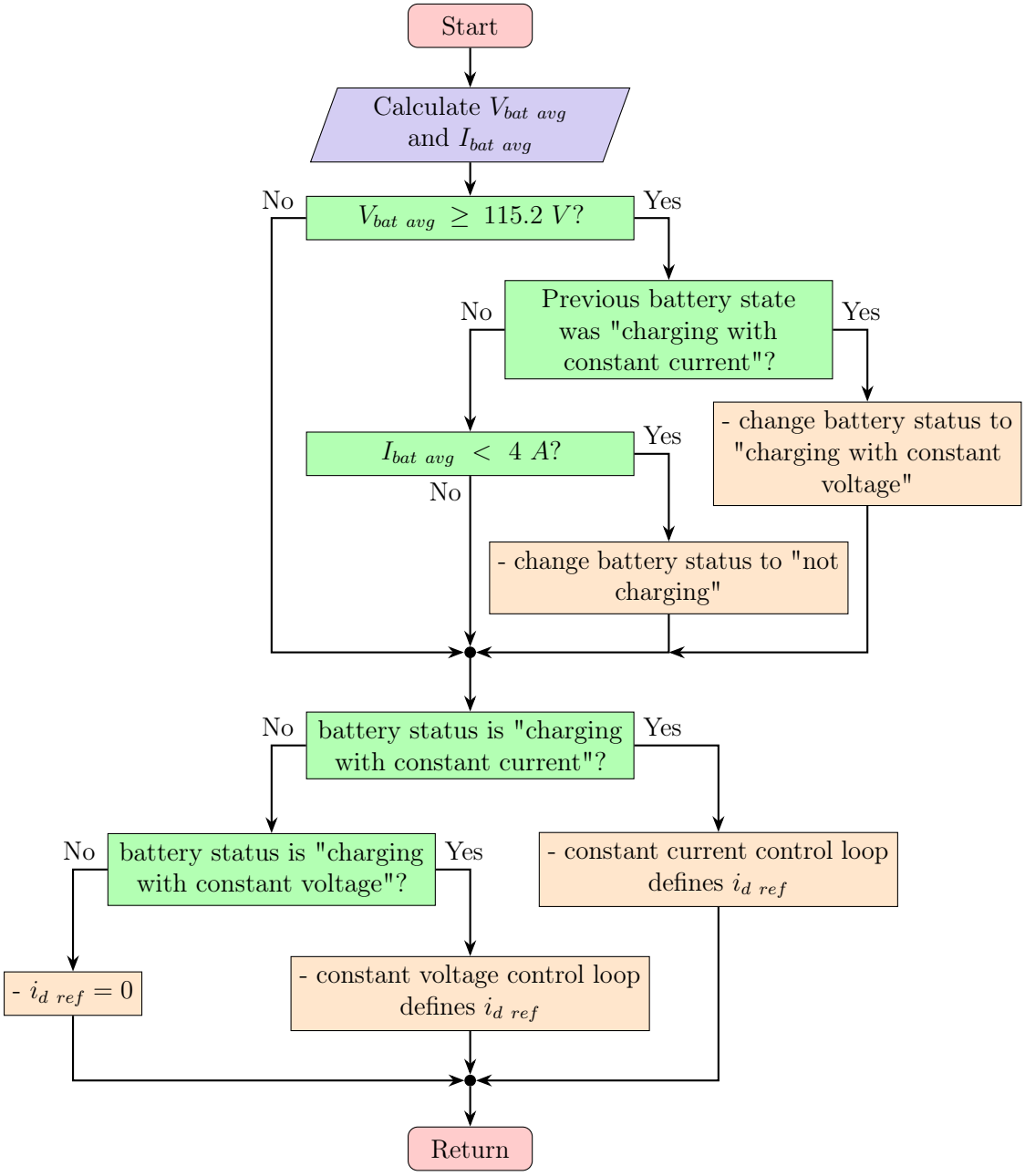
The routine that selects the controller is summarized in the flowchart shown in Figure 38. First, the routine calculate the average voltage and current of the batteries

($V_{bat\ avg}$ and $I_{bat\ avg}$). Then verifies if the battery has reached 115.2 V. If yes, the routine checks if the previous battery charging state was "charging with constant current". The battery state can be either "not charging", "charging with constant current" or "charging with constant voltage". So, if the battery was "charging with constant current", the battery status is switched to "charging with constant voltage". If not, the routine checks if the current $I_{bat\ avg}$ is below 4 A. If yes, this means that the charging process has ended or that it was not charging, so the status is changed to "not charging". After defining the charging status, the battery charge routine chooses which controller should be used to calculate $i_{d\ ref}$, or if the value is zero (not charging).

Figure 38 – Flowchart of battery charge routine



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3.3.5.3 Reactive power controller

The reactive power controller estimates the load reactive power consumption at the fundamental frequency by summing the reactive power sourced by the grid and the reactive power delivered by the inverter. The reactive power from the grid is calculated through Equation 3.6, while the reactive power from the inverter results from multiplying i_q for the nominal power. Then, the controller sets the inverter current to provide the same reactive power required by the load, with a maximum defined in the converters' main routine. Equation 3.7 shows the logic employed.

$$i_{q\ ref} = \frac{Q_{load}}{S_{nom}} \tag{3.7}$$

3.4 Conclusion

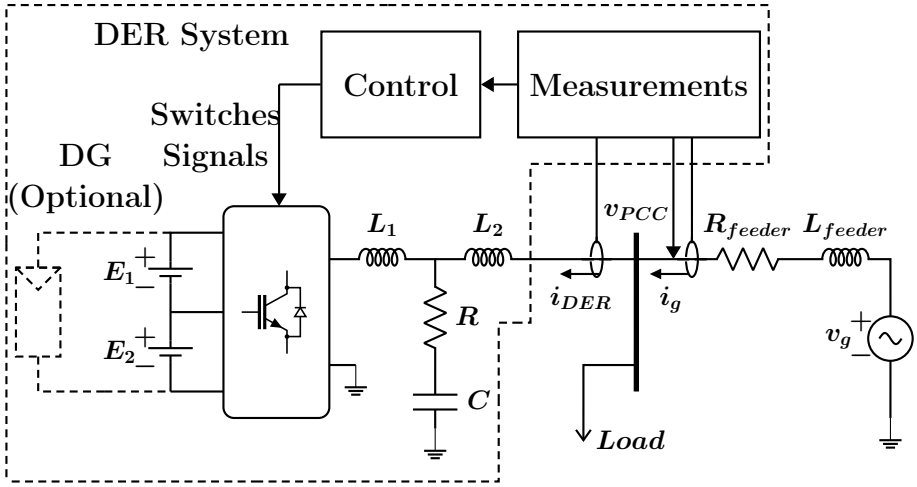
This chapter described the Typhoon HIL simulation setup and the control system implemented in the eZdsp F28335 used in this project. The longest part focuses on the routines programmed in the microcontroller, providing details on control loops, parameter values, and the logic of operation of the converter. It is worth mentioning that the controllers' parameter values were consulted in the literature and then adjusted based on the system response. For this work, the control of the converter operation is through the debugging tool of Code Composer, and a user interface is not implemented yet.

4 Results and Discussion

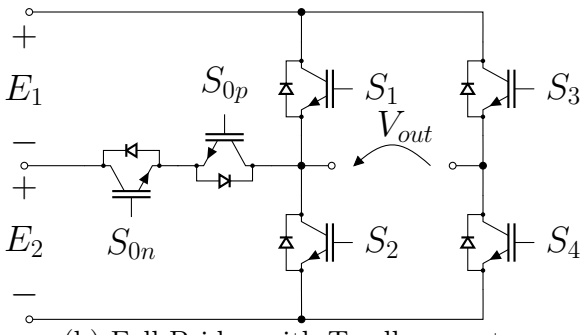
This chapter presents some results of HIL simulations of the systems described in chapter 3. First, the results from functions of the fundamental operation of the inverter (PWM, SOGI, PLL, and the current controller) are presented and discussed. Then, results from the operation modes with functions of STATCOM, harmonic compensation, battery charge, and power export are analyzed. Additionally, the force discharge mode and operation with multiple functions are shown.

The structure of the simulated system, as well as the five-level single phase inverter, were presented in Chapter 2, but are repeated here in Figures 39a and 39b to facilitate visualization.

Figure 39 – Simulated system and five-level inverter



(a) DER system



(b) Full-Bridge with T-cell converter

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4.1 PWM, SOGI, PLL and Current Controller

At first, the system is operating in idle mode - no active nor reactive power exchange. The inverter synthesizes the fundamental V_{PCC} waveform. The test result details the switches signals received by Typhoon HIL from the controller's PWM. Samples are collected by typhoon HIL at the simulation step size of 1 μs. Figure 40 shows the pulses read by typhoon HIL over a cycle, and Figure 41 presents a zoom when the sine changes from the positive semi-cycle to the negative semi-cycle. It is possible to see that the dead time applied in the PWM configuration was enough to allow the switches to change states without short-circuiting any converters' leg. The voltage output and grid voltage are shown in Figure 42. During semi-cycles changing, all IGBTs are turned-off for a short moment and depending on the current direction, it forces the polarization of the IGBT's diodes, causing $E_1 + E_2$ or $-E_1 - E_2$ voltage output for a short time of up to the dead time value. As mentioned in section 3.3.2.2, the dead time is of 2 μs, as one switch turns off 1 μs earlier than the calculated time and the next switch turns on 1 μs after. Since the frequency is high, this pulse is filtered and does not interfere with the converter's overall performance.

Figure 40 – Switches signals read by Typhoon HIL over one grid cycle

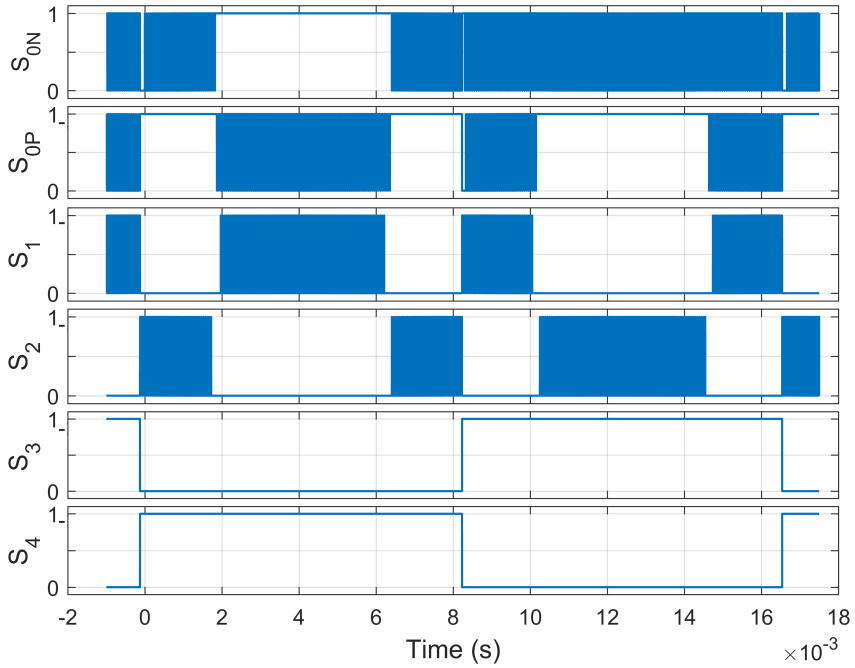

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Figure 41 – Switches signals during a semi-cycle change

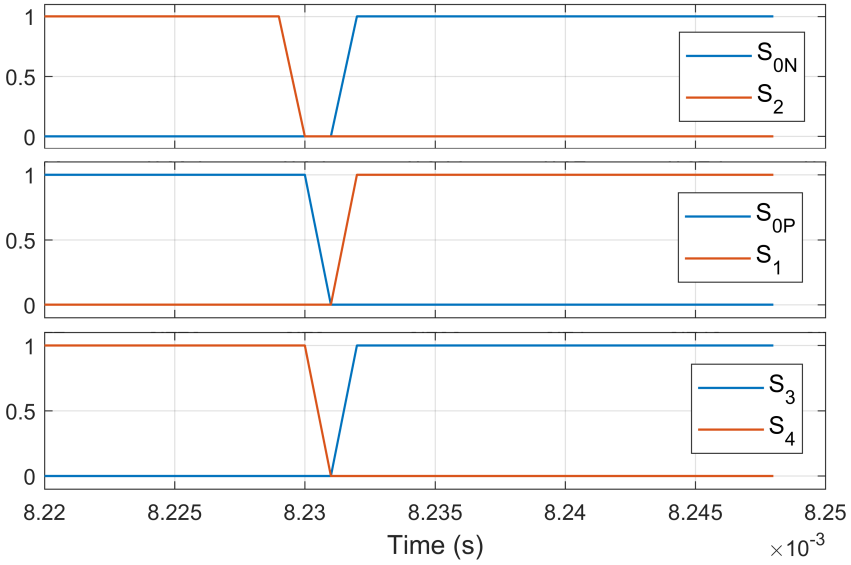

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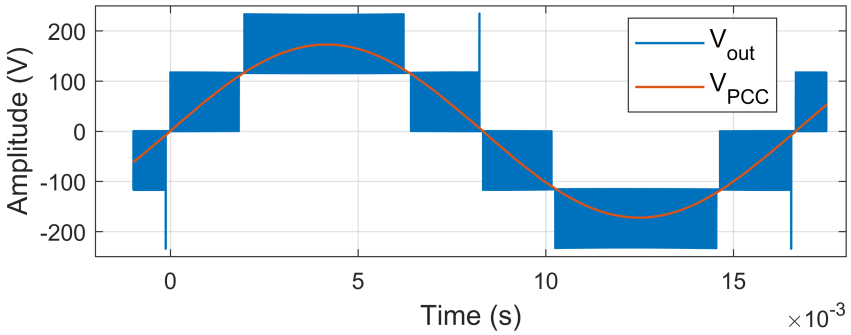
Figure 42 – Converter's voltage output and voltage at the point of common coupling



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Then, tests were made to evaluate SOGI and PLL performance, with samples collected at 10.8kHz from the eZdsp. Figure 43 shows $V_{PCC\ \alpha}$ and $V_{PCC\ \beta}$, Figure 44 depicts the angle θ that results from the PLL, and Figure 45 presents $V_{PCC\ d}$ and $V_{PCC\ q}$. From Figure 43, $V_{PCC\ \alpha}$ and $V_{PCC\ \beta}$ have a sinusoidal shape, and $V_{PCC\ \beta}$ lags $V_{PCC\ \alpha}$ by 90^o. The angle θ observed in Figure 44 behaves as expected, ramping up cyclically from 0 to 2π radians at 60 Hz. From Figure 45, the d component of the voltage oscillates with an amplitude of around 0.037 pu, from 0.9376 to 0.975 pu, and $V_{PCC\ q}$ is very close to zero.

In the following tests, steps from 0 to 0.5pu in $i_{d\ ref}$ and $i_{q\ ref}$ were applied to evaluate the current controllers' performance (0.5 pu is about 15.75 A_{RMS}). It is worth mentioning that these tests require the storage of more variables, and the hardware memory accessed through code composer is limited. Therefore, it was necessary to adopt a slower sample rate for data acquisition than in the tests of the SOGI and PLL. Samples were collected at 1.92 kHz. Figure 46 shows the behavior of i_d and i_q in the eZdsp when a step

Figure 43 – $V_{PCC\ \alpha}$ and $V_{PCC\ \beta}$ generated by the SOGI

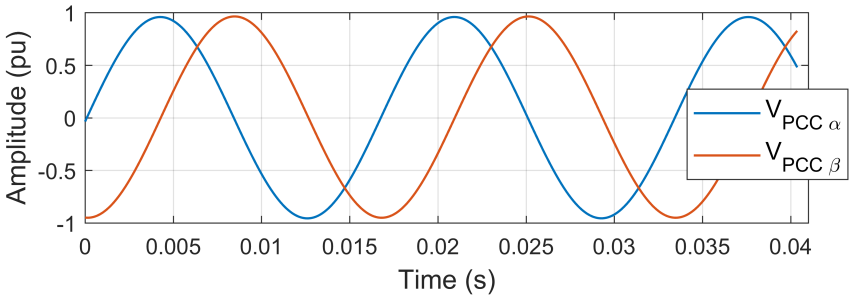

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Figure 44 – θ angle tracked by the PLL

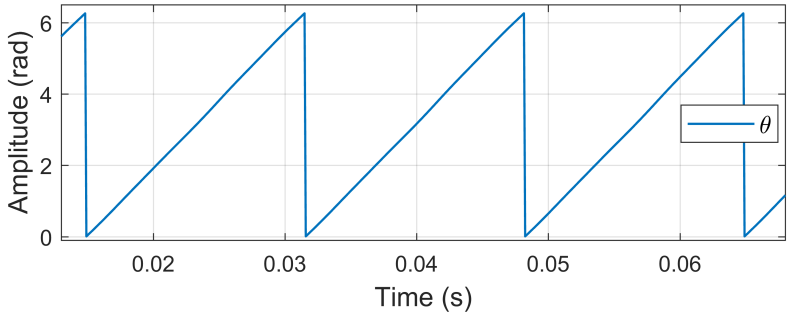

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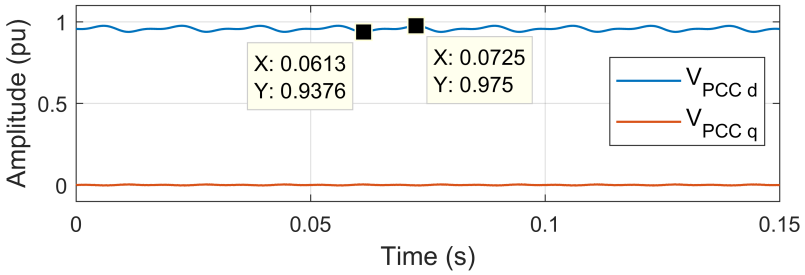
Figure 45 – $V_{PCC\ d}$ and $V_{PCC\ q}$



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in $i_{d\ ref}$ is applied. Figure 47 presents the grid's current i_g, the converter's current i_{DER}, and the voltage V_{PCC} in Typhoon HIL. For this test, a heavy R load was connected.

It is observed, through Figure 46, that the i_d loop takes about 0.03 s (around two grid cycles) to stabilize and that i_q is also disturbed when $i_{d\ ref}$ changes, suggesting that the control loops are still slightly coupled. The converters' current in the *abc* frame of Figure 47 shows that the reference transition was smooth, and no significant disturbance in v_{PCC} was perceived.

Figure 46 – i_d and i_q behavior during step in $i_{d\ ref}$

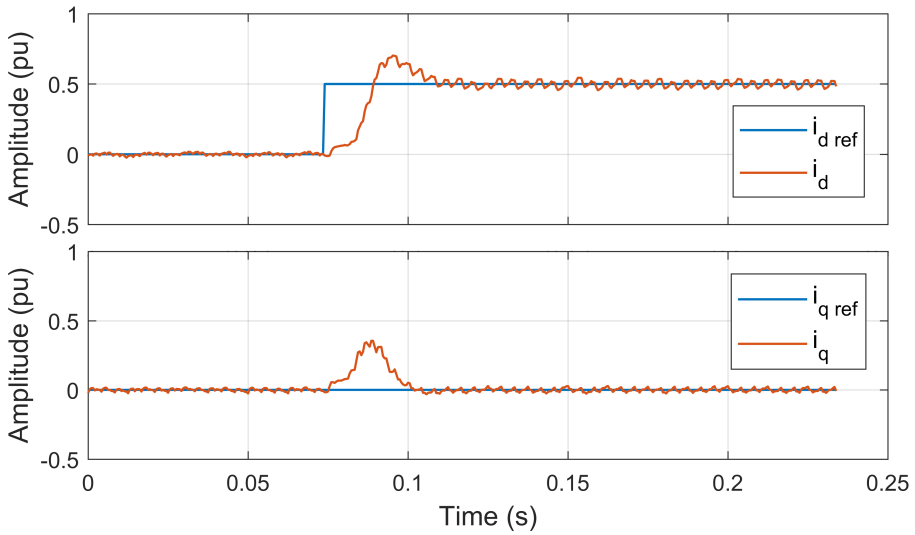

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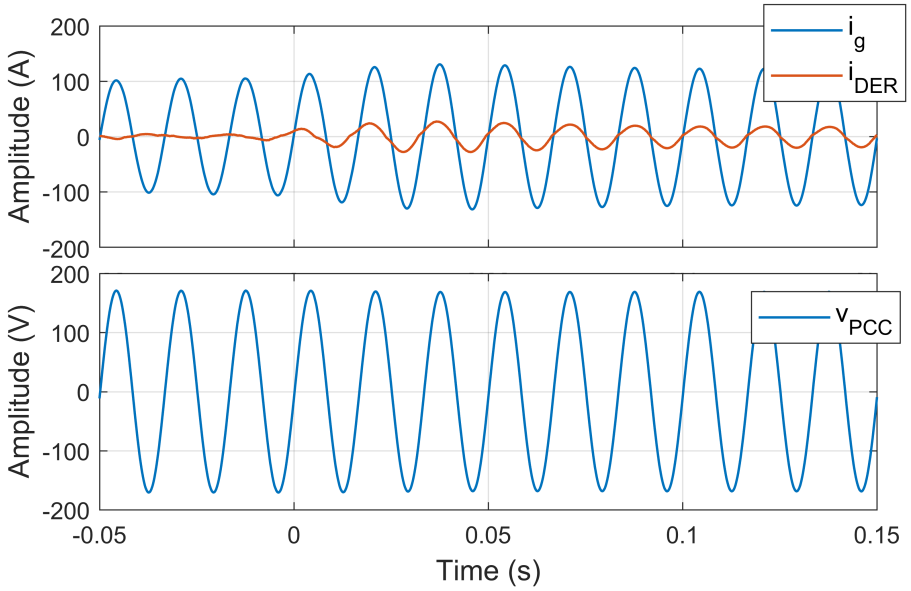
Figure 47 – i_g and i_{DER} behavior during step in $i_{d\ ref}$



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The results for a step in $i_{q\ ref}$, shown in Figures 48 and 49, are similar to the step change in $i_{d\ ref}$. From i_{DER} in Figure 49, it can be observed the STATCOM is acting as a capacitor.

Figure 48 – i_d and i_q behavior during step in $i_{q\ ref}$

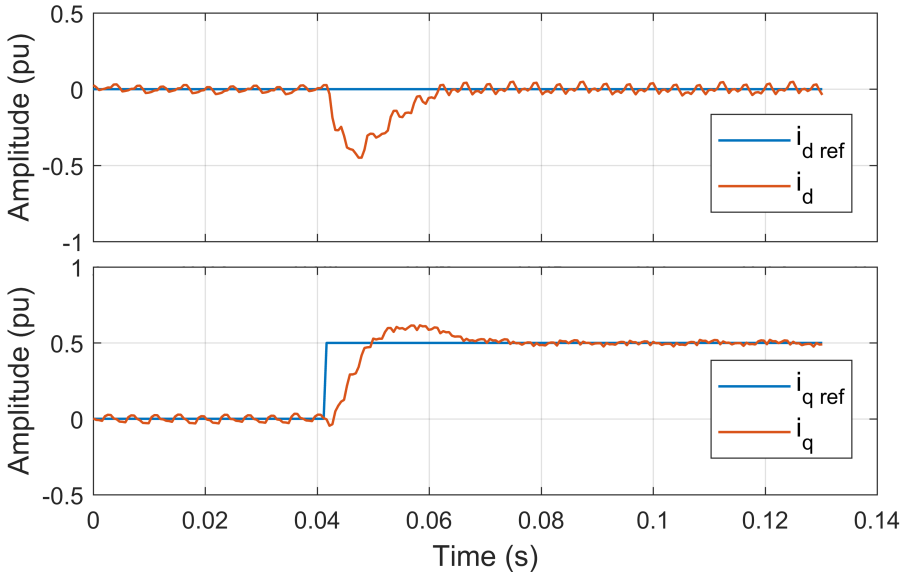

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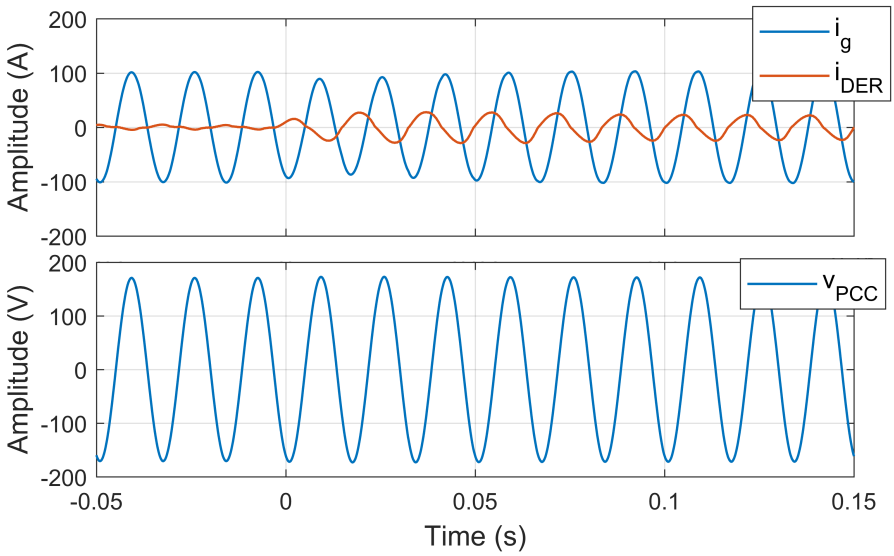
Figure 49 – i_g and i_{DER} behavior during step in $i_{q\ ref}$



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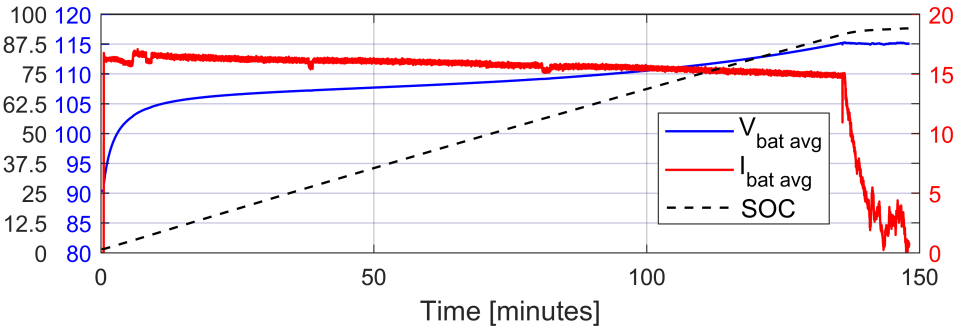
4.2 Battery Charge Mode

A charging cycle was tested, and the results are in Figure 50. These results are collected in Typhoon HIL. The initial State Of Charge (SOC) was very low, at 1.5%, and the average battery voltage was around 92 V. The charging process starts with the constant current controller imposing a peak value of about 17 A that reduces slowly to an end value of 15 A. Then, after the voltage reaches 115 V, the voltage controller keeps charging the battery, and the current reduces fast. The voltage controller maintains the voltage at 115 V, and the final batteries' SOC was around 94%. This test reveals that the

current controller is not robust, as it was supposed to keep the current constant at 16 A. On the other hand, the voltage controller can control the voltage very close to the desired value. The charging time is around 2h30min, and a light R load was connected during this test.

Figure 50 – Battery charge test results



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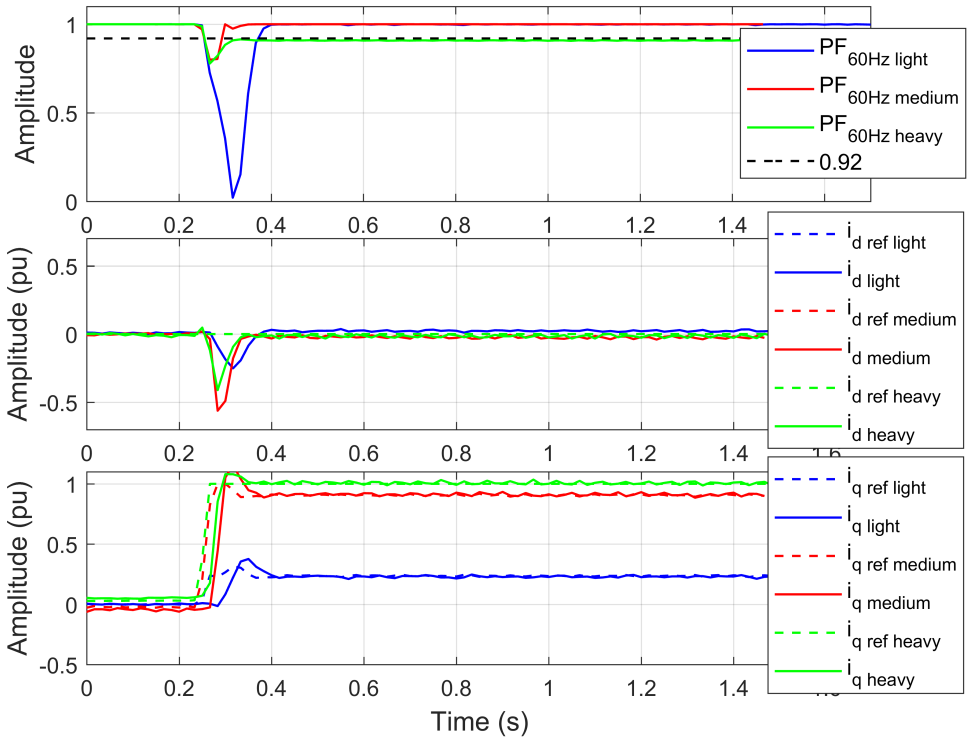
4.3 STATCOM Mode

For testing STATCOM mode (flowchart of Figure 27), several load changes were applied, and samples of the current and power factor were collected at 60 Hz using the software Code Composer, which allows to program the microcontroller and access its variables. Voltage and current in typhoon HIL was also monitored. The load intensity is not changed within a test unless explicitly mentioned. Therefore, a light R to RL load change implies that both R and RL loads are of light intensity, for example. Since the Power Factor (PF) limit in Brazil is 0.92, a black dashed line with this reference value is shown in the graphs of PF. No active power flow was realized ($i_{d\ ref} = 0$).

Figure 51 shows the PF at the fundamental frequency and the i_d and i_q currents of the converter for an R to RL load change. In light and medium loads, the PF at the fundamental frequency is raised to 1.0. However, with the heavy load, it stays around 0.92 because the converter reaches its maximum power compensation capacity. Light R to RL load change has the slowest response time, but none of the cases displayed here needed more than 0.2 s to reestablish the PF.

Figure 52 presents the test results for RL to RC load changes. For the heavy load, the converter changes from the maximum capacitive behavior to the maximum inductive behavior. The capacitive load has a 1Ω pre-charge resistor, removed 0.4 s after the load change. With the light load, its removal disturbance is not visible in the graphs, but with the medium load, it can be observed in the i_q graph through a slight negative increase in the current around the time of 0.62 s. With the heavy load, the resistor removal is observed

Figure 51 – R to RL load change test results



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through a decrease in PF, around 0.62 s. In the results presented here, the converter also can increase the PF within less than 0.2 s after the load change.

In the following tests, load changes are from RL to rectified load, and Figure 53 shows the results. It is observed in the figure that the converter absorbs some reactive power ($i_q < 0$) when the rectified load is connected, indicating that this load has a capacitive behavior in the fundamental frequency. The PF is raised in less than 0.2 seconds in this test too.

The behavior of voltage at the connection point (v_{PCC}) and currents of the grid (i_g) and of the DER (i_{DER}) during the heavy RL to heavy RC load change is shown in Figure 54. The moment of the removal of the pre-charge resistor is observed in Figure 55. The load change and the pre-charge resistor removal disturb the grid current and voltage, but the system recovers fast. Similar disturbances are observed during the other load changes, but the one shown in Figure 54 has a higher relevance, since the capacitor connection is similar to a momentaneous short-circuit in the operation.

Figure 52 – RL to RC load change test results

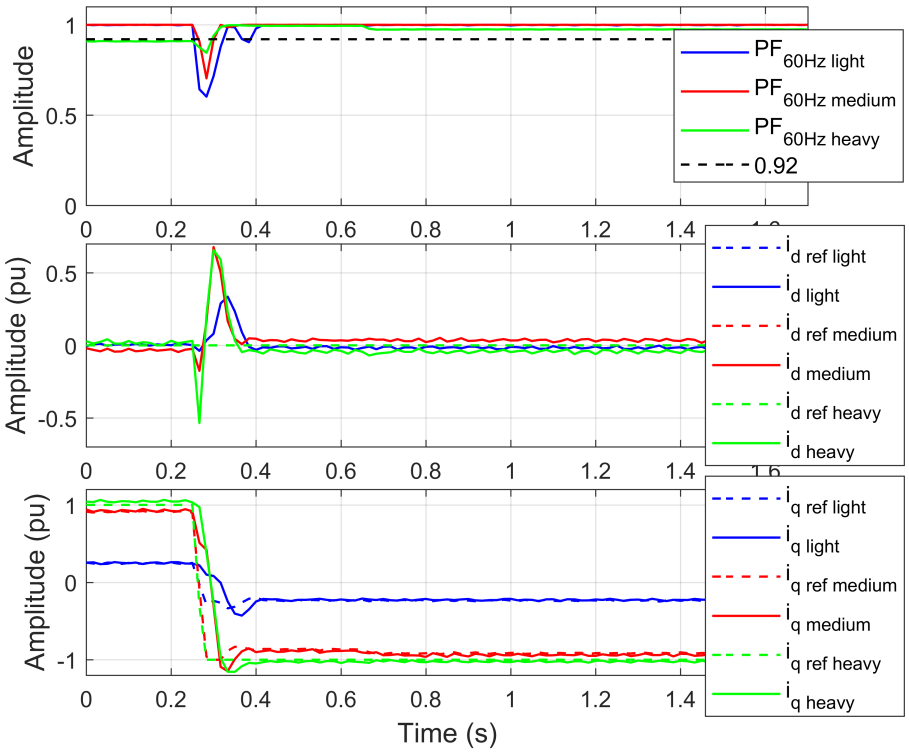

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Figure 53 – RL to rectified load change test results

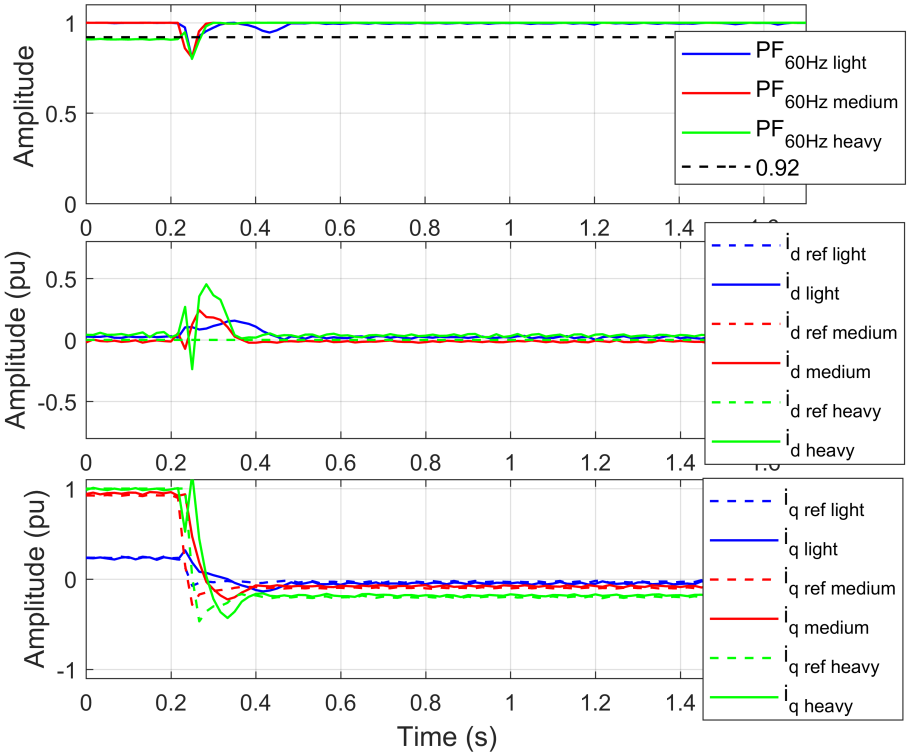

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Figure 54 – Heavy RL to RC load change (Typhoon HIL)

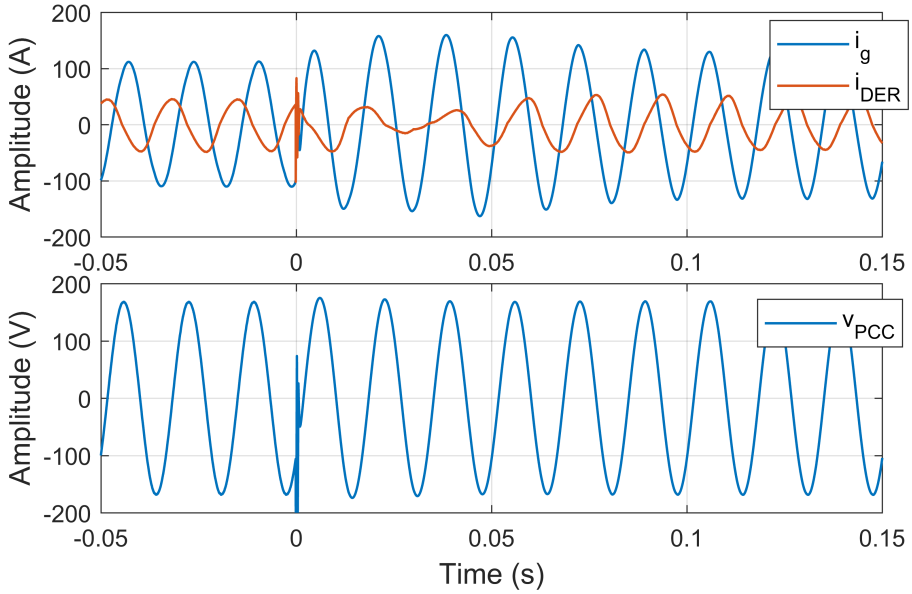

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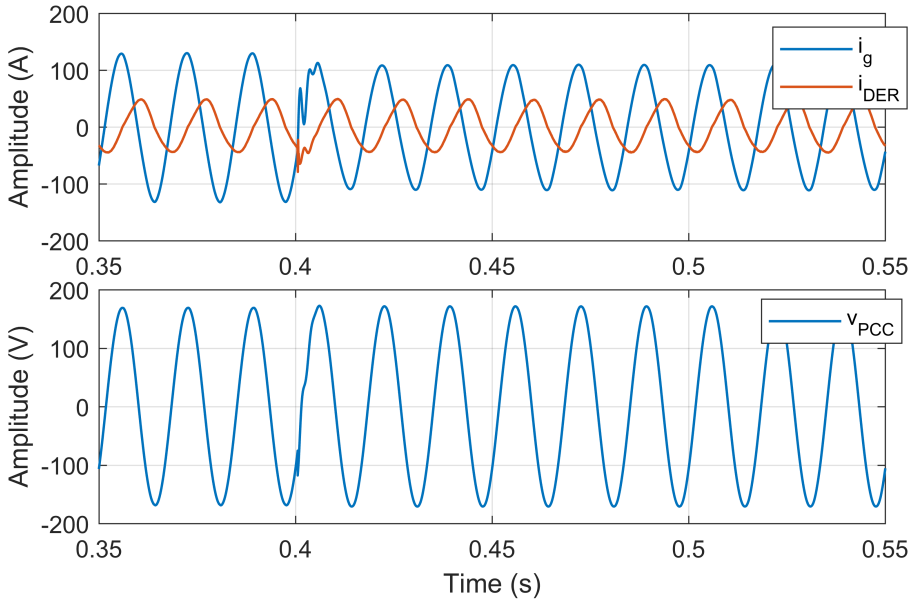
Figure 55 – Heavy RC load, pre-charge resistor removal



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4.4 Harmonic Compensation Mode

The waveform of the grid voltage and current and the converters' current when operating with the heavy rectified load and without the harmonic compensation (the DER is fluctuating) is exposed in Figure 56. Figure 57 displays the spectrum of the currents and reveals that odd harmonics up to the 9th are present in the grid current. Five seconds of samples were collected through Typhoon HIL at a 1 MHz sampling rate.

Figure 56 – Current and voltage waves without compensation

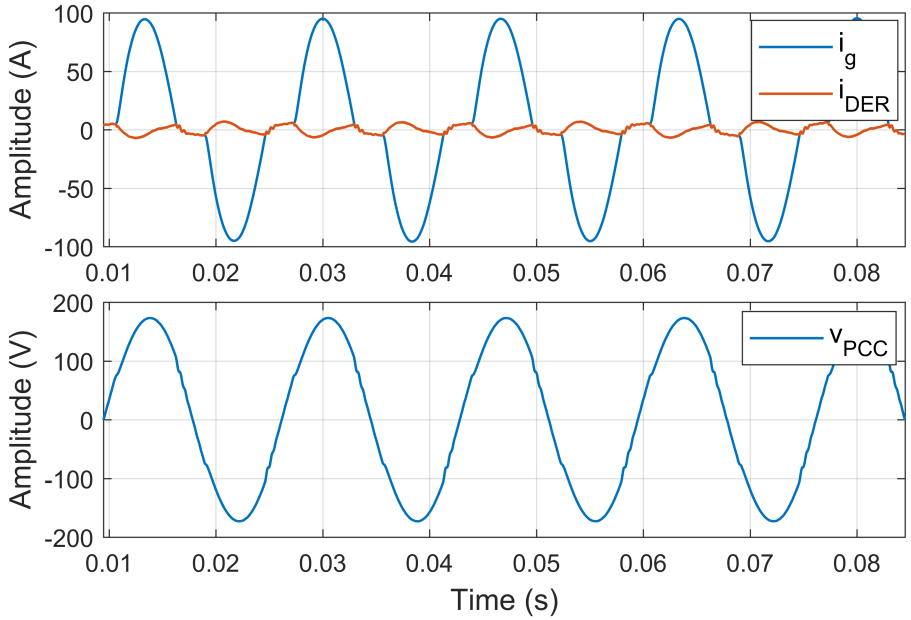

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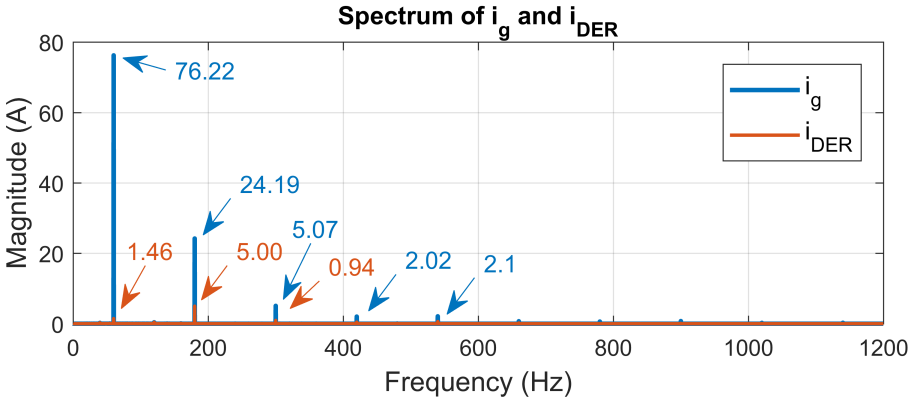
Figure 57 – Current spectrum without compensation



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After activating the harmonic compensation, the waveform acquires a more sinusoidal shape, and the 3rd, 5th, and 7th order harmonics in the grid current are compensated by the DER system. Figure 58 depicts the waveform with compensation, and Figure 59

shows the grid and DER currents spectrum. The results show that the harmonic compensation strategy is effective.

Figure 58 – Current and voltage waves with compensation

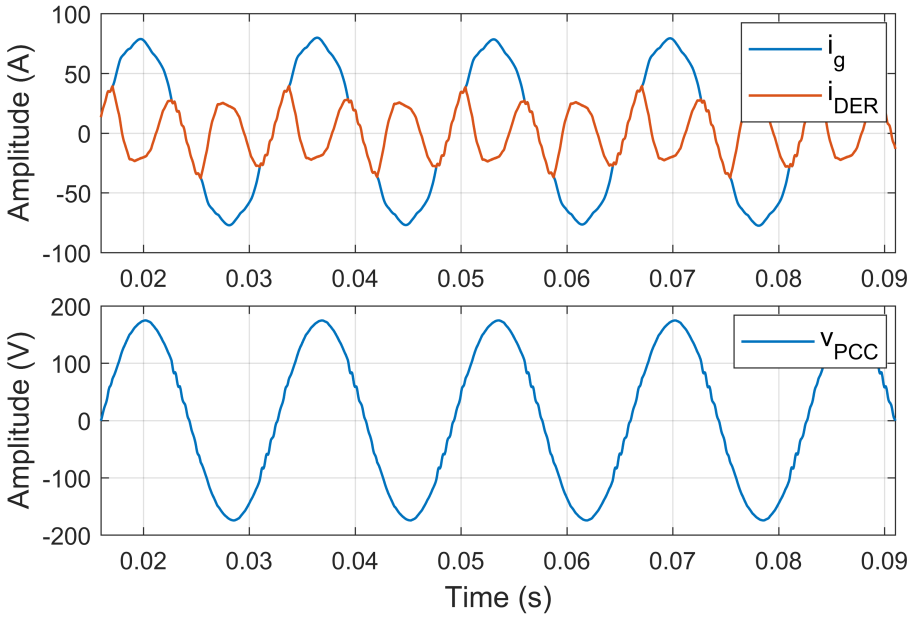

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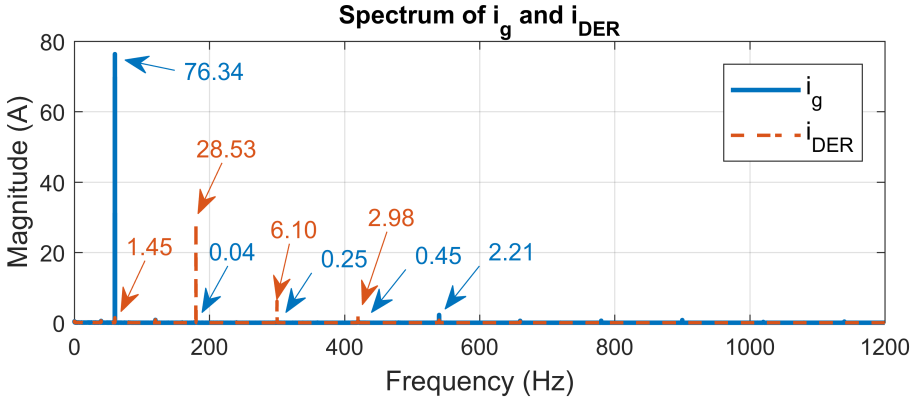
Figure 59 – Current spectrum with compensation



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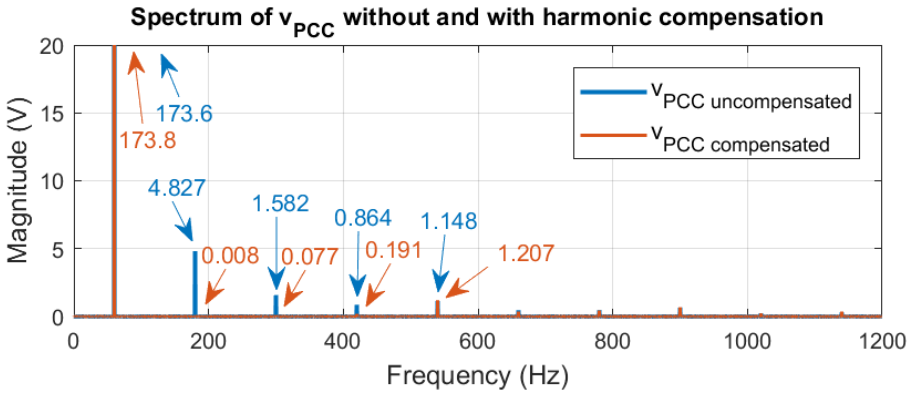
The harmonic content reduction of the current reflects in the voltage at the connection point, reducing also its harmonic content, once the grid current is more sinusoidal. The Figure 60 shows the spectrum of v_{PCC} without and with the compensation and it is observed a reduction in the magnitudes of 3rd, 5th, and 7th order harmonics in v_{PCC}.

Figure 60 – Voltage spectrum without and with compensation



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A load change was applied to evaluate the behavior of the harmonics. In this test, the system starts with a heavy rectified load and then switches to a heavy R load. The measured dq currents of the 3rd, 5th, and 7th harmonics are shown in Figure 61, collected from the DSP. The behavior of the voltage at the connection point (v_{PCC}) and grid (i_g) and DER (i_{DER}) currents, obtained from the HIL circuit, are shown in Figure 62. A steady-state error is observed in the grid current harmonic components in dq. But the controllers' actuation during the load change is fast, and the DER current reduces after removing the non-linear load.

Figure 61 – Harmonic currents dq components behavior during load change

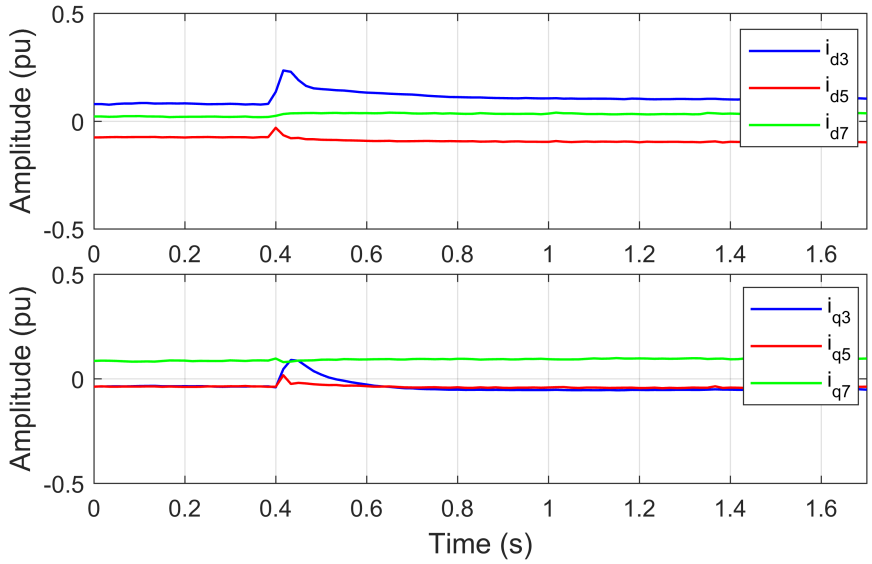

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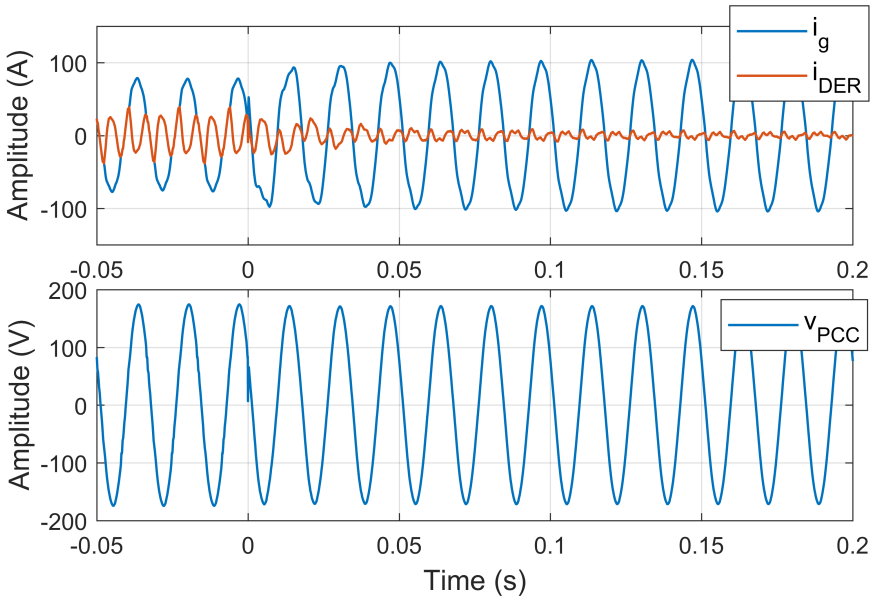
Figure 62 – i_g, i_{DER} and v_{PCC} behavior during load change with harmonic compensation



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The last test of the harmonic compensation mode evaluates the behavior of the harmonics' *dq* current when harmonic compensation turns on. Figures 63, 64, and 65 show the *dq* currents for the light, medium, and heavy rectified loads.

Figure 63 – Grid harmonic current behavior when compensation is turned on (light rectified load)

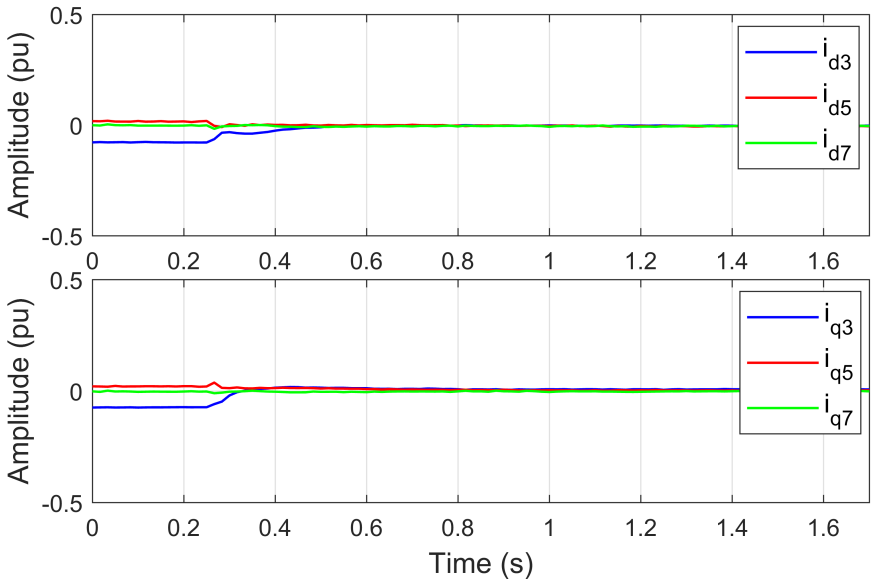

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Figure 64 – Grid harmonic current behavior when compensation is turned on (medium rectified load)

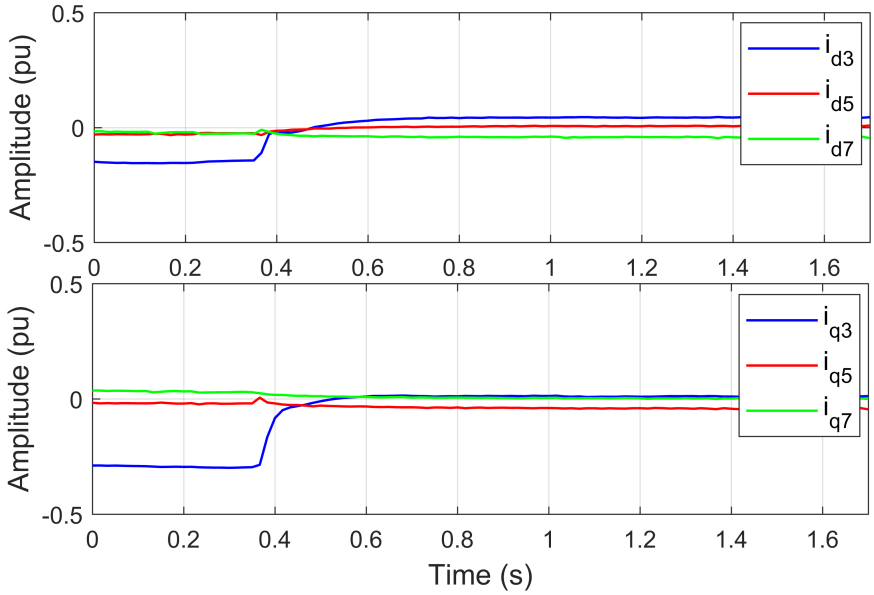

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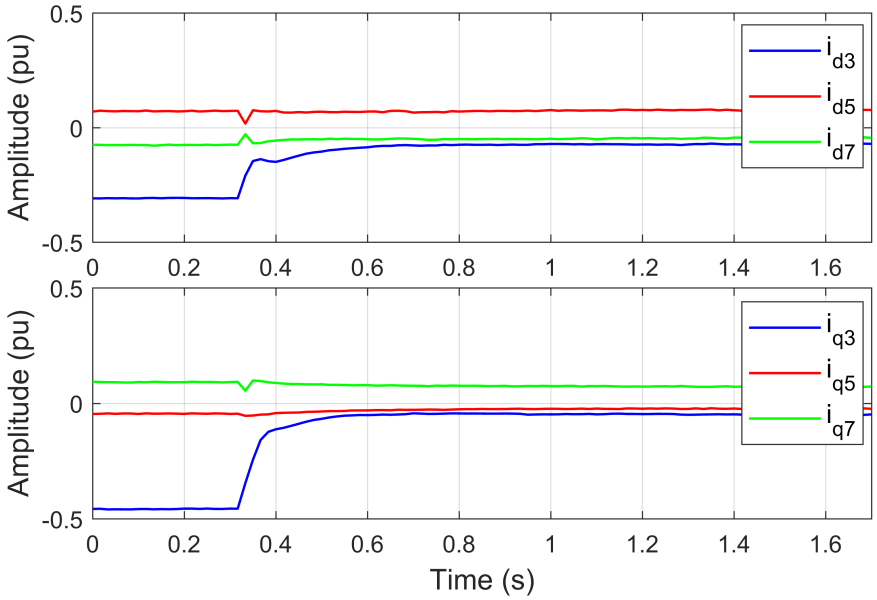
Figure 65 – Grid harmonic current behavior when compensation is turned on (heavy rectified load)



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The third harmonic has the highest value in all three cases, and the controller reduces it. Although *dq* currents of the 5^{th} and 7^{th} harmonics do not seem to have relevant changes, these components reduce in the current spectrum. To exemplify this, Figure 66 shows the spectrum of the currents without compensation for the medium rectified load, while Figure 67 presents the spectrum after compensation. Figure 68 depicts the behavior of the currents in the time domain when compensation turns on.

Figure 66 – Spectrum of the currents with compensation off (medium rectified load)

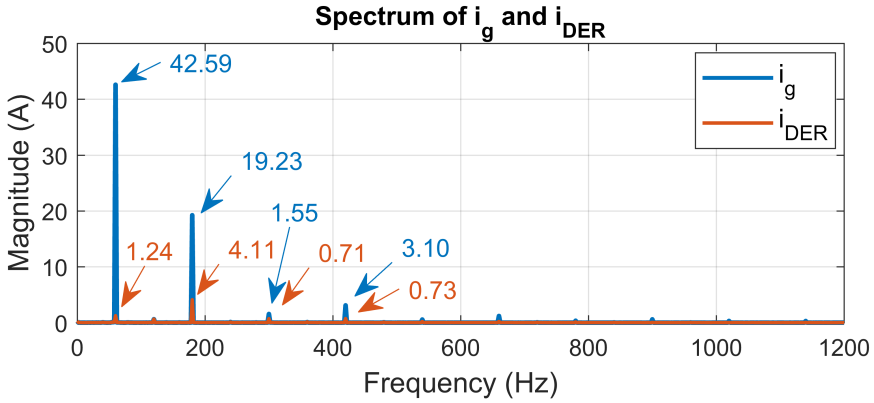

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Figure 67 – Spectrum of the currents with compensation on (medium rectified load)

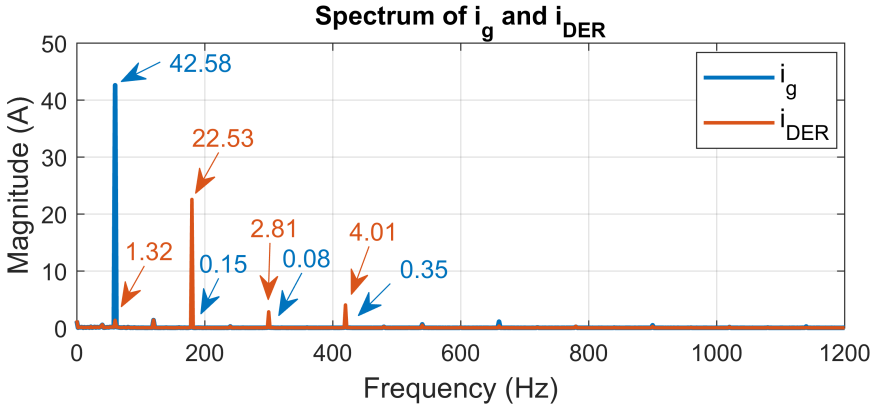

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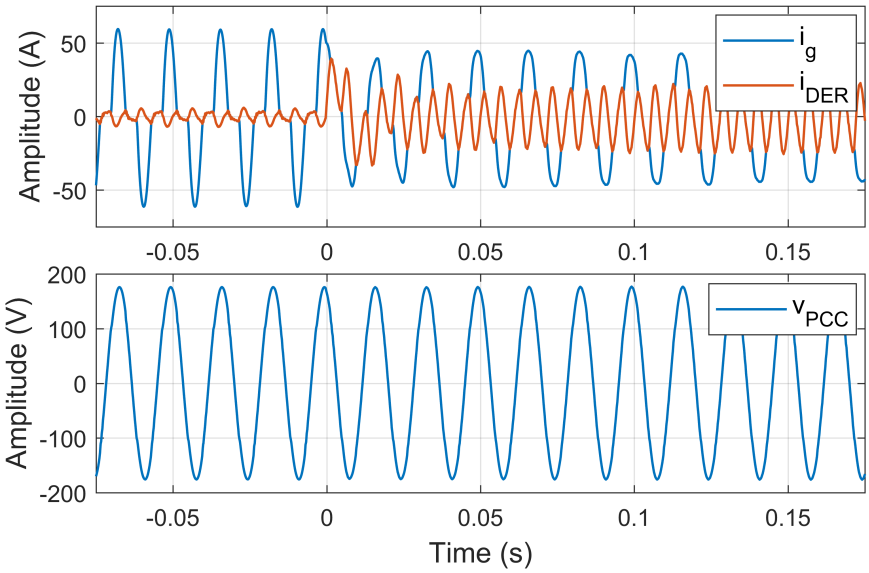
Figure 68 – i_g, i_{DER} and v_{PCC} when compensation turns on (medium rectified load)



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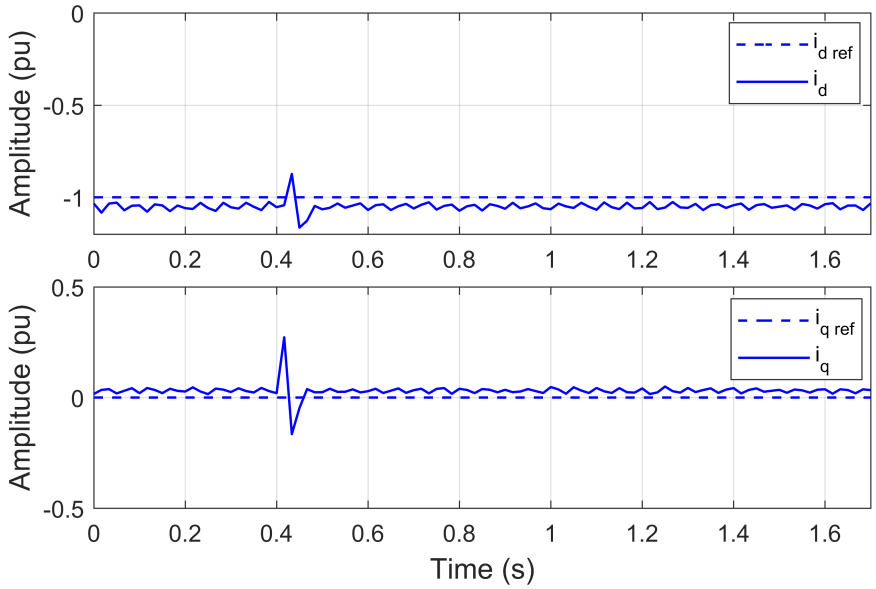
4.5 Power export mode

In the power export mode (flowchart of Figure 29), priority is given to send energy from batteries to grid. The converter is operating with a heavy R load connected to the PCC. At 0.4 s, a change to a heavy RL load occurs. Figure 69 shows the converters' i_d and i_q currents collected in the software code composer during the load change, and Figure 70 shows the current and the voltage acquired from Typhoon HIL. Since the converter power capacity focuses on exporting power, after a fast transient reaction the control keeps i_d high while i_q is low.

Figure 69 – *dq* currents during load change in power export mode



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4.6 Forced discharge mode

The next test exemplifies the automatic mode change that occurs when the batteries' voltage gets too high. An electrical source is connected to the batteries at 0.3 s, to simulate an external power source feeding them. The converter is initially in STATCOM mode with a heavy RL load, but when the voltage of the batteries reaches 118 V, it switches to the forced discharge mode, turning off the STATCOM function. Figure 71 shows the mean voltage and current of the batteries, and Figure 72 depicts the *dq* currents. When the operation mode changes, $v_{bat\ avg}$ ramps down to around 116 V, and the batteries slowly discharge. The discharge current grows fast to about 17 A and keeps floating around this value.

Figure 70 – i_g, i_{DER} and v_{PCC} during load change in power export mode

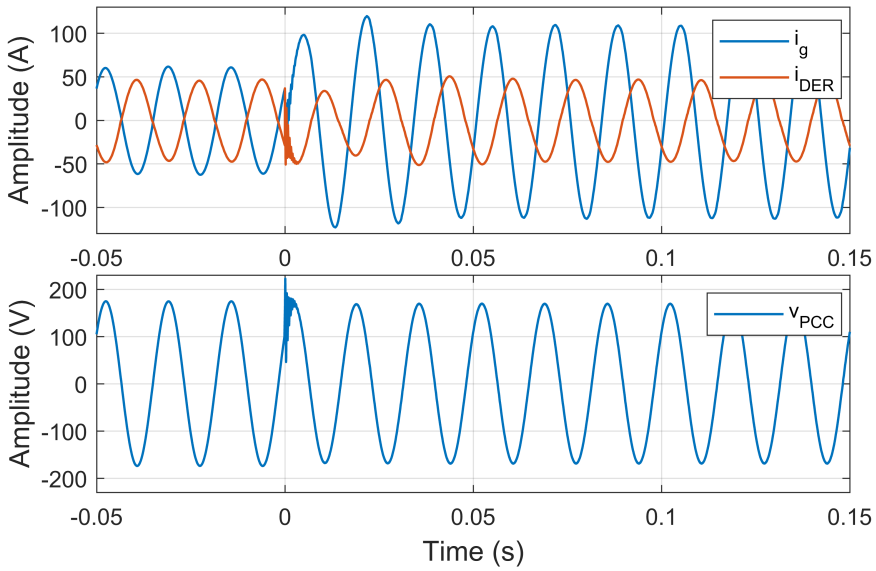

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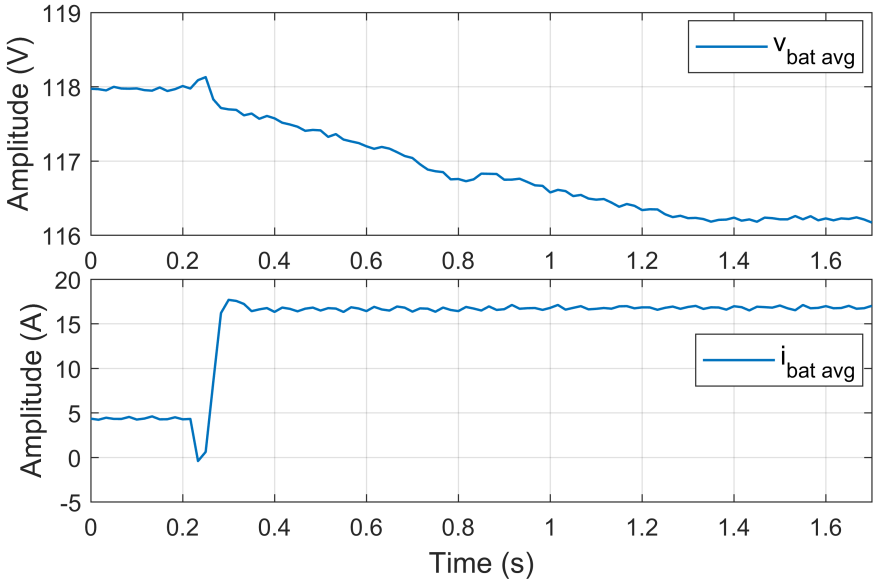
Figure 71 – Batteries' Voltage and Current when changing to force discharge mode



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After discharging the batteries until that $v_{bat\ avg}$ reaches 112 V, the converter switches back to the STATCOM mode. The behavior of the batteries' voltage and current when switching back to STATCOM mode is presented in Figure 73, while Figure 74 shows the behavior of the DER's *dq* currents. Right after the mode change, $v_{bat\ avg}$ raises to 113 V, and $i_{bat\ avg}$ reduces and stays close to zero.

Figure 72 – *dq* currents when changing to force discharge mode

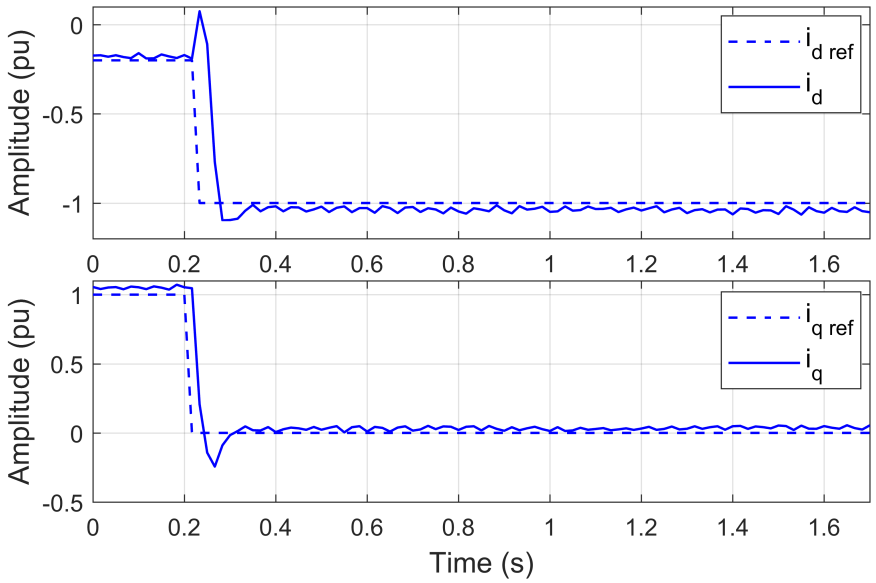

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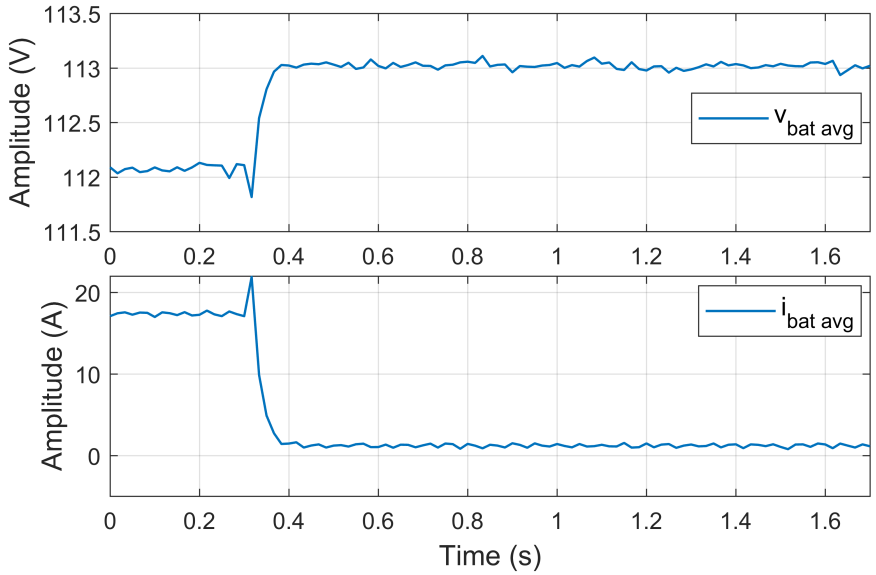
Figure 73 – Batteries' Voltage and Current when changing back to STATCOM mode



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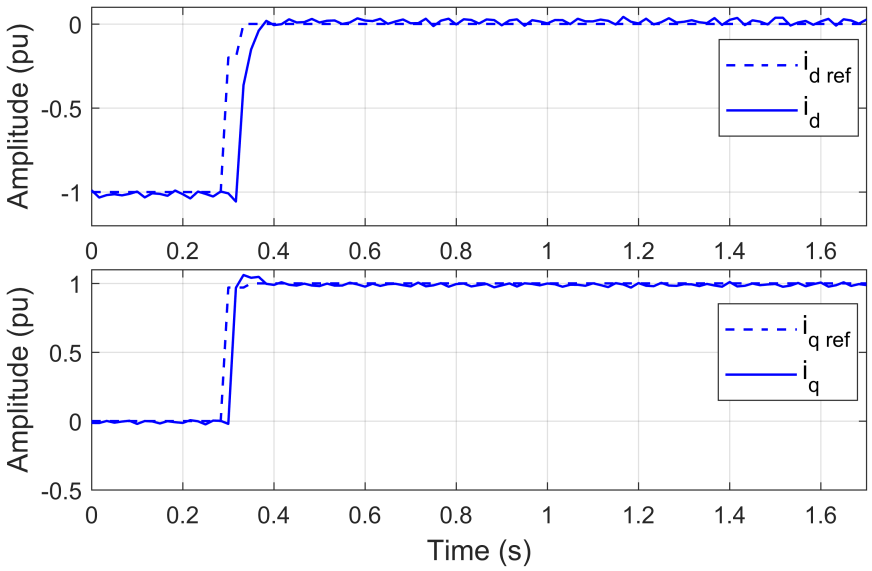
4.7 Simultaneous functions

This section presents the results of tests with simultaneous functions activated in an operation mode. STATCOM and harmonic compensation are activated while in battery charge mode. The battery is considered already fully charged, so in flowchart of Figure 26 the decision results in $i_{d\ max} = 0.3$ and $i_{q\ max} = 0.958$. The load changes from heavy RL to heavy rectified load. Figure 75 shows the power factor and the *dq* currents. Figure 76 depicts the waveform of the currents and voltage. Since the battery is at full

Figure 74 – dq currents when changing back to STATCOM mode



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charge, $i_{d\ ref}$ is zero through the test, and the controller directs the power capacity to i_q. When the load changes, i_q reduces due to the capacitive nature of the load. Also, the converter compensates harmonics, being the third one the most prominent considering single-phase rectifiers. Another effect observed is a reduction in i_d without a command in $i_{d\ ref}$, configuring a steady state error.

Figure 75 – PF and dq currents in battery charge mode, with STATCOM and harmonic compensation activated

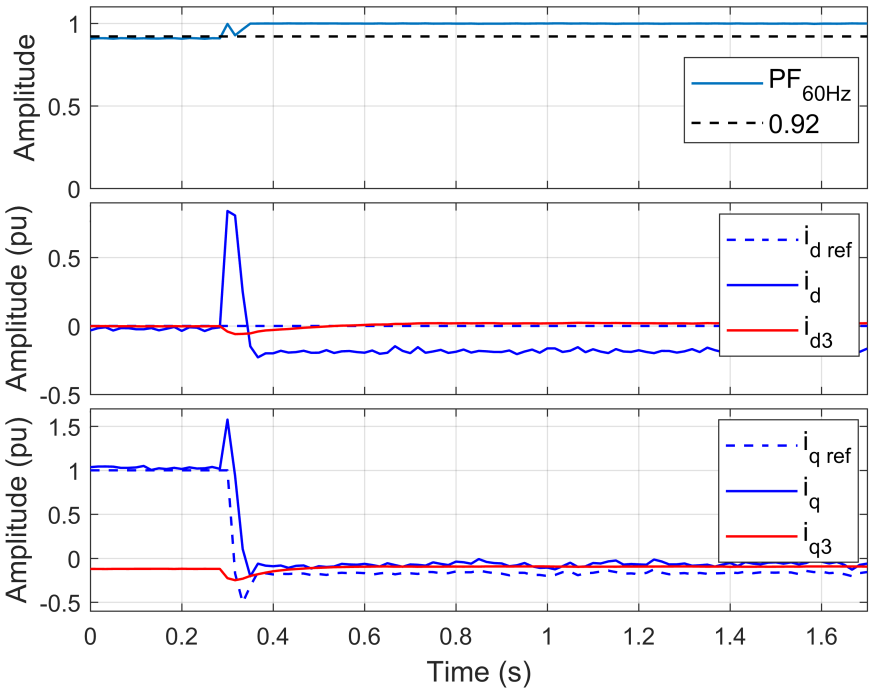

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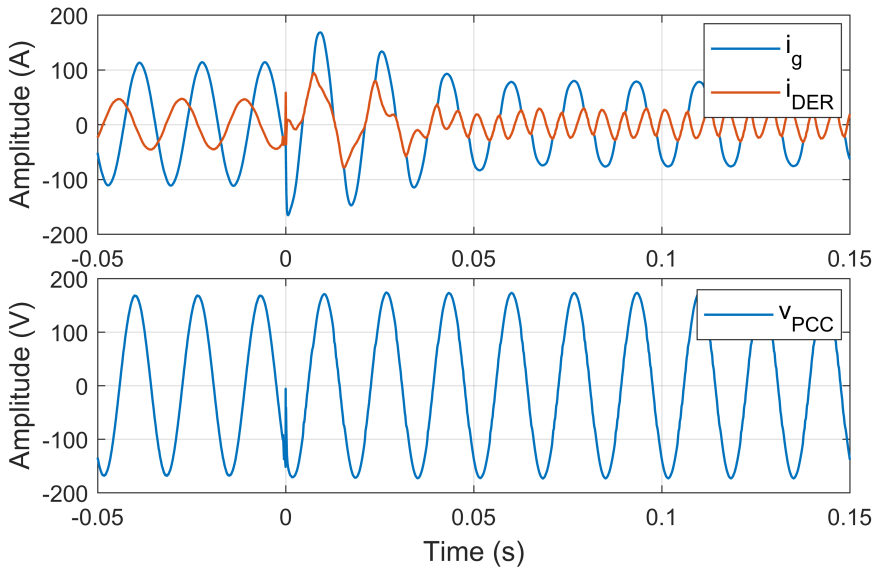
Figure 76 – i_g, i_{DER} and v_{PCC} in battery charge mode, with STATCOM and harmonic compensation activated



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The next test is considering operation in STATCOM mode, with the functions of battery charging and harmonic compensation activated. The PF and *dq* currents are shown in Figure 77, and the current and voltage in the *abc* frame are in Figure 78. Initially, the system has a heavy RL load connected, and the converter dedicates to PF correction. When the load changes to heavy rectified load, $i_{q\ ref}$ reduce, and part of the capacity is free to charge the battery, so $i_{d\ ref}$ increases. The converter also compensates for some of the load's harmonics, and there is a steady state error in i_d and in i_q.

The harmonic compensation mode is also tested with the functions of STATCOM and battery charging activated. Figure 79 depicts the PF and *dq* currents, while Figure 80 presents the currents and voltage in the *abc* frame. Since the system focuses on harmonic compensation, the converter injects some reactive power to increase PF. But, it is not enough to raise it above the Brazilian limit of 0.92. When the load changes from heavy RL to heavy rectified, $i_{q\ ref}$ reduces and PF increases. However, a steady state error also appears in i_d and in i_q.

At last, the power export mode with the STATCOM function is tested. Figure 81 shows that PF is below the limit. It happens because the converter focuses on supplying active power and sends only a small portion of reactive power, while the grid furnishes more reactive power and less active power. When the load changes, i_q current diminishes, and PF increases. The harmonic compensation does not activate because the DER's RMS current is close to the limit. Figure 82 depicts the current and voltage in the *abc* frame.

Figure 77 – PF and *dq* currents in STATCOM mode, with battery charge and harmonic compensation activated

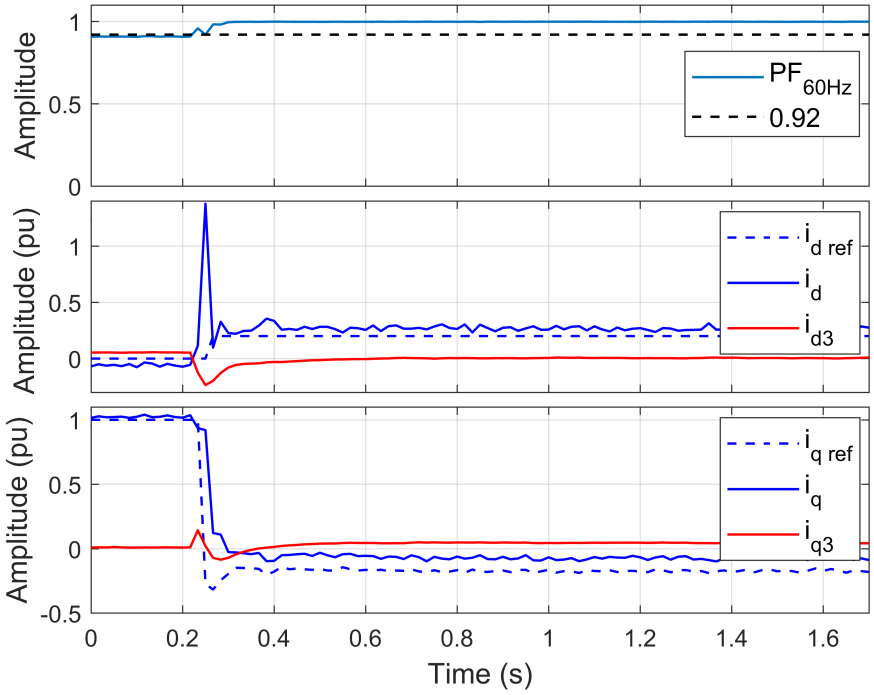

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Figure 78 – i_g, i_{DER} and v_{PCC} in STATCOM mode, with battery charge and harmonic compensation activated

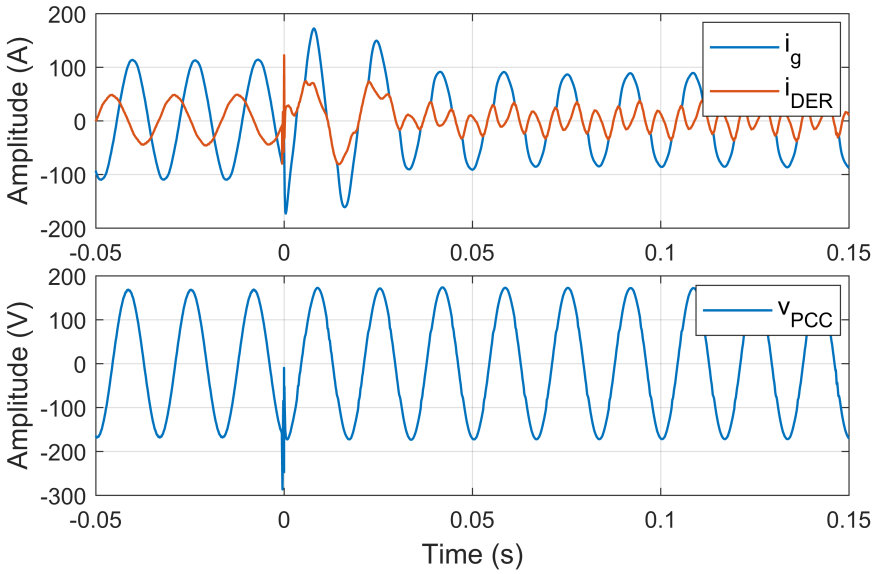

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Figure 79 – PF and *dq* currents in harmonic compensation mode, with battery charge and STATCOM activated

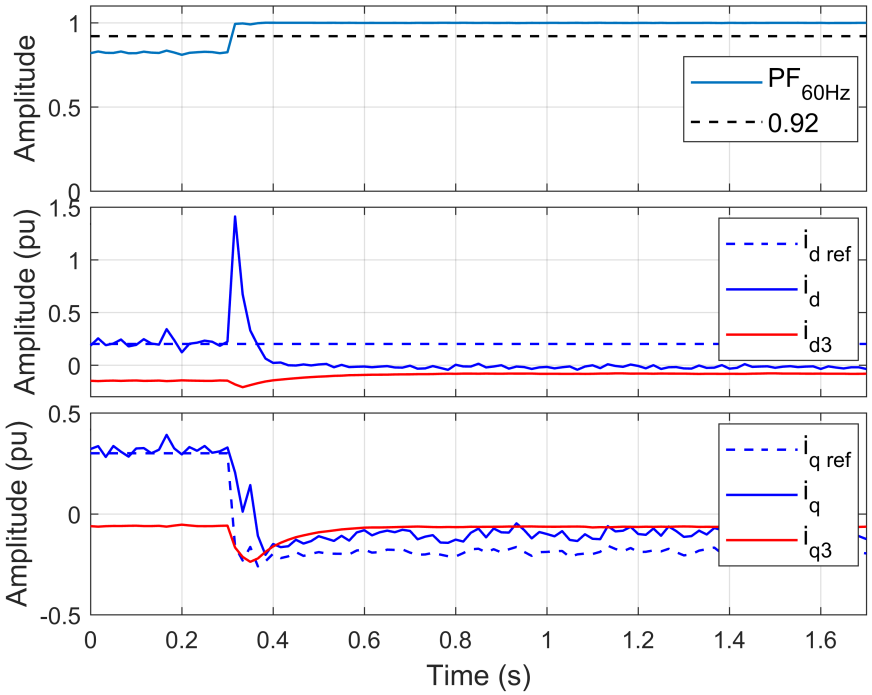

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Figure 80 – i_g, i_{DER} and v_{PCC} in harmonic compensation mode, with battery charge and STATCOM activated

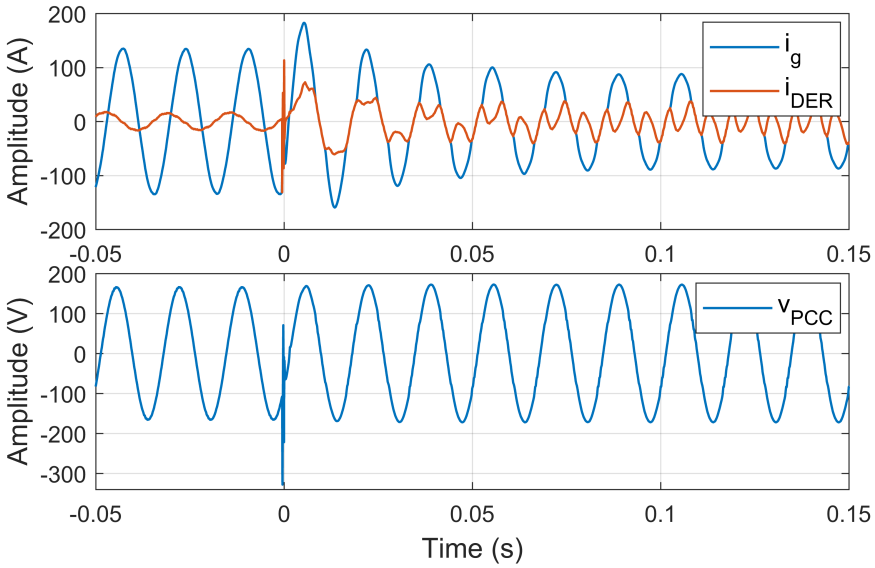

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Figure 81 – PF and *dq* currents in power export mode, with STATCOM function activated

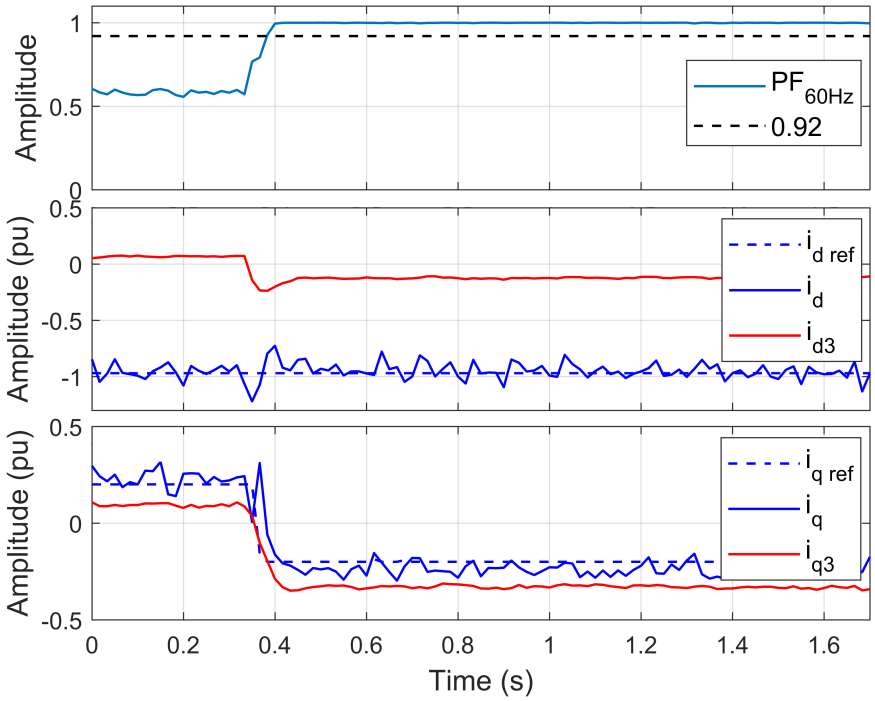

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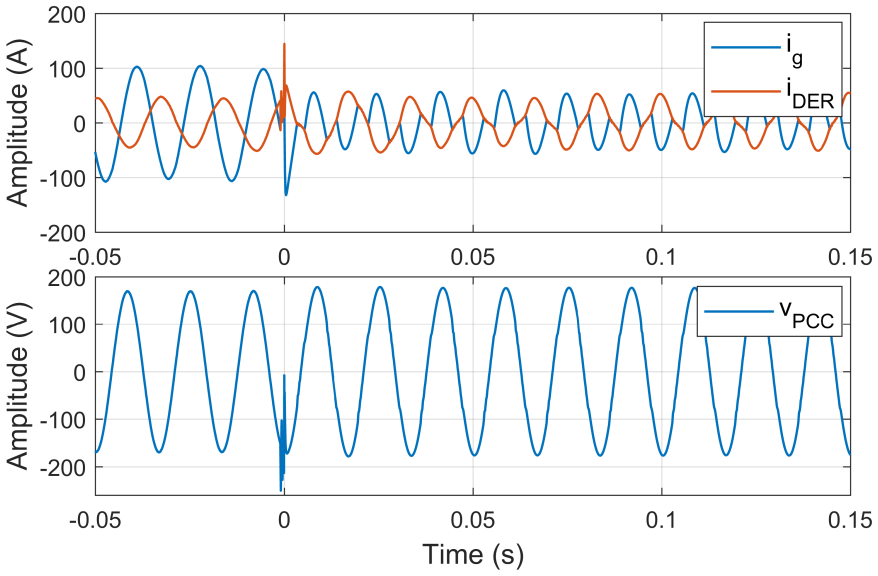
Figure 82 – i_g, i_{DER} and v_{PCC} in power export mode, with STATCOM function activated



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4.8 Conclusions

This Chapter presented results from several HIL experiments, with the eZdsp F28335 sending control signals to Typhoon HIL 402 and receiving measurements from Typhoon HIL. Initially, results of the essential functions of the DC-AC converter were shown (PWM, SOGI, PLL, and current control loop). Afterward, the results from tests with the operation modes and simultaneous functions were presented.

As for the PWM, the pulses are received in typhoon HIL, and the dead time of 2 μs adopted is enough to prevent short circuits in the converter's legs. The voltage output from the converter has five levels and, after being filtered, has a clean sinusoidal shape, as shown in Figure 42. This voltage sometimes has undesired $\pm$200 V pulses in place of 0 V when changing positive or negative semi-cycles. Those pulses last up to 2 μs and occur because all switches are open for the dead-time duration. On such occasions, the converter's current forces the conduction of some of the reverse diodes of the IGBTs.

The SOGI's outputs are $v_{PCC\ \alpha}$ and $v_{PCC\ \beta}$, presented in Figure 43. They have a clean sinusoidal shape and are separated by 90^o, as expected. The PLL output the angle used in $\alpha\beta$ to dq transforms employed in the control algorithm. θ have the expected behavior, ramping up from 0 to 2π radians, and $v_{PCC\ q}$ is close to zero while $v_{PCC\ d}$ is close to 1, with an 0.04 pu oscillation amplitude.

Steps in i_d and i_q references showed that the current controller adjusts the current in around 0.03 seconds for a step in i_d or in i_q when connected to the heavy R load. Also, the interference between i_d and i_q loops indicates a small coupling between the control loops.

The converter battery charge mode can charge the batteries from a SOC of 1.5% to 94% in 2h30min. The average constant current reference in the first part of the charging is 16 A, and the results showed that it started with 17 A and diminished a bit over time, ending with 15 A instead of staying constant. In the constant voltage part of the charging, the voltage stayed at 115.2 V. These results reveal that the constant current controller might need some adjustments if an exact charging current is required, but the overall performance is good.

STATCOM operation results indicate that the converter can correct the PF for the loads tested, reaching its maximum current capacity when connected to heavy RL and RC loads. With heavy RL, PF stays close to 0.92. Meanwhile, with the heavy RC load, PF gets close to 1.0. In the load changes shown, PF correction occurred in about 0.2 s.

The efficiency of the harmonic compensation strategy is observed when comparing the current spectrum without and with the harmonic compensation. A steady state error appears in the dq harmonic currents indicating that the converter was not compensating that harmonic component. However, this is not observed in the spectrum, as the compen-

sated harmonics are small. This effect is not further investigated in this project since the compensation in *abc* frame is achieved regardless of the steady-state error in the *dq* frame.

The power export mode results show that it focuses on delivering active power as designed. The forced discharge mode activates when the batteries' voltage is too high, and the previous operation mode is activated when the voltage reaches a safe value.

At last, the results from simultaneous functions activated show that the converter can operate with multiple functions. However, when harmonic compensation is activated, a steady state error may appear in the DER's *dq* currents, and this behavior requires further investigation. A curious fact is that the error did not affect the system's PF correction.

5 Conclusion and future work

5.1 Conclusion

As the number of DC-AC converters connected to the grid increases, it becomes more interesting that these devices also provide power grid support functions. Motivated by the benefits of power quality and the increased value that these functions bring to the DER, this dissertation presented the control logic design of a DC-AC converter with STATCOM and harmonic compensation functions, besides active power export and battery charging. This work's main contribution is the detailed design of the control logic of the converter, having the algorithm implemented on an eZdsp F28335 is tested through HIL simulations.

Chapter 2 presented a theoretical background with a literature review that helped define the control strategies and subroutines adopted. The control loops, parameters chosen, and flowcharts of the logic implemented were further detailed in Chapter 3, together with the power system description simulated.

The simulation results were shown in Chapter 4 and revealed good performance with some space for improvements. The PWM pulses have enough dead time and don't short circuit. SOGI outputs $v_{PCC\ \alpha}$ and $v_{PCC\ \beta}$ have a clean sinusoidal shape and are 90^o apart. The angle θ tracked by the PLL is also well behaved. The current controllers designed have a response time of about 0.03 s for steps in the references $i_{d\ ref}$ and $i_{q\ ref}$. The converter is able to monitor the batteries voltage and automatically adjust its operation to charge or discharge the batteries when reaching critical voltage levels. When in STATCOM mode, the DER is able to effectively adjust the PF in about 0.2 s, and the converter can compensate for harmonics in the grid's current, consequently contributing to reduce harmonic content in the voltage at the point of common coupling and raising power quality.

At last, it is worth mentioning that the objectives proposed in this dissertation were achieved. The results show that the DC-AC converter can effectively support the grid with PF correction and harmonic compensation while managing the batteries' voltage and charging batteries or exporting power when required. This operation brings additional value to DERs and contributes to grid confiability and energy quality.

5.2 Further Works

Since this work did not explore a user interface, many contributions can be made to increase the equipment value and complement this work. One idea is to establish a wireless

communication for the converter and develop a supervisory system that can monitor the grid conditions and set the converter operation mode according to what is best for both DC and AC grids. The supervisory can also choose the best time to charge the batteries or when to export power, flattening the energy demand of the AC loads served (peak shaver), saving cost with improvements to the power system infrastructure, and raising the installation load factor. Additionally, the converter can be required to charge the batteries when energy cost is cheaper and to export energy when it is expensive.

Parameters of several control loops were set based on an initial guess from the literature consulted and improved with adjustments according to the results of the simulations. An improvement suggestion is to use a detailed model for the inverter or optimization algorithms in the test data to find the best parameters and achieve a more robust operation of the equipment. Moreover, when operating with harmonic compensation simultaneously with other functions, a steady state error in *dq* currents appears. Therefore, an investigation to explain this behavior is encouraged.

Another possibility is to incorporate in the control the operation as a Virtual Synchronous Generator (VSG).

5.3 Publications

Two papers were publish as a result of studies performed during this master's course and are listed below.

RIBEIRO, L. S.; SALLES, J. L. F.; FARDIN, J. F. F.; SIMONETTI, D. S. L. Detecção de Ilhamento Através da Estimação da Impedância de Linha Utilizando Mínimos Quadrados Recursivo (in English: Island Detection Through Grid Impedance Estimation Using Recursive Least Squares). In: *XXIV Congresso Brasileiro de Automática*. Fortaleza, 2022.

RIBEIRO, L. S.; SIMONETTI, D. S. L. Voltage-Controlled and Current-Controlled Low Voltage STATCOM: A Comparison. In: *International Conference on Renewable Energy and Power Quality (ICREPQ'22)*. Vigo, 2022.

Other three papers were published with results of studies performed previous to the master's course enrollment, but also relate to the development of this project and are listed below.

RIBEIRO, L. S.; SIMONETTI, D. S. L. Projeto e Simulação de um Controlador Fuzzy para BT-STATCOM Monofásico (in English: Design and Simulation of a Fuzzy Controller for Single-Phase LV-STATCOM). In: *XXIV Congresso Brasileiro de Automática*. Fortaleza, 2022.

RIBEIRO, L. S.; SIMONETTI, D. S. L. Aplicando Perturba & Observa para Controle de Fator de Potência por BT-STATCOM Monofásico (in English: Applying Perturb & Observe to Power Factor Control by Single-Phase LV-STATCOM). In: *Anais da XIV Conferência Brasileira Sobre Qualidade da Energia Elétrica*. 2021.

RIBEIRO, LAILA SINDRA; SIMONETTI, DOMINGOS SAVIO LYRIO . Evaluation of Three Control Aproaches for a Single-Phase Low-Voltage STATCOM. In: *2021 IEEE PES Innovative Smart Grid Technologies Conference Latin America (ISGT Latin America)*. Lima, 2021.

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Annex

ANNEX A – Typhoon HIL 402 Specifications

HIL402 technical details.

Processor		Up to 4 cores
Analog I/O	Channels	16 inputs / 16 outputs
	Resolution	16 bit
	Voltage range	± 10 V
	Sample rate	1 MSPS
	Protection	± 24 V tolerant, ESD protection
	Connector	DIN 41612, type C, 96 pin male connector
Digital I/O	Channels	32 inputs / 32 outputs
	Threshold voltages (DI)	$V_{IL(max)}$ = 0.8 V; $V_{IH(min)}$ = 2.0 V
	Threshold voltages (DO)	$V_{OL(max)}$ = 0.2 V; $V_{OH(min)}$ = 4.8 V
	Input resistance	10 kΩ
	Protection	± 24 V tolerant, ESD protection
	Connector	DIN 41612, type C, 96 pin male connector
Externally available power supply	± 5 V analog	up to 1 A, resettable protection
	± 12 V analog	up to 0.5 A, resettable protection
	3.3 V digital	up to 1 A, resettable protection
	5 V digital	up to 1 A, resettable protection
Connectivity	USB	2.0 high speed, B-type connector
	Ethernet	RJ45 connector
Compatibility	HIL DSP interface	
	HIL uGrid DSP interface	
	HIL Breakout board	
	HIL dSpace interface board	
Power supply	External	100 - 250 VAC, ≥ 60 W

ANNEX B – Batteries Specifications

Contents

1 pc- RE-START Battery (though sizes may differ, operation will be the same for all models).
2 pcs -Wireless Keyfobs to remotely turn ON the RE-START (built-in Jump Starting) feature.

RE-START BATTERY

WIRELESS KEYFOBS

Specifications

BATTERY TYPE:	Lithium Iron-Phosphate (LifePo4) with built-in Battery Management System
VOLTAGE:	12.8V (nominal)
CAPACITY:	24-80 Ah (see battery label)
CRANKING AMPS:	1000-2000 peak (see battery label)
DIMENSIONS:	(varies per model)
WEIGHT:	8-25 lbs (varies per model)
MAX CHARGING RATE:	20 Amps
MAX CHARGING VOLTAGE:	14.6V
CHARGER TYPE:	Lithium-Iron Phosphate for 12.8V Batteries

ANNEX C – TMS320F28335 Features and Functional Block Diagram

TMS320F28335, TMS320F28335-Q1, TMS320F28334, TMS320F28333
TMS320F28332, TMS320F28235, TMS320F28235-Q1
TMS320F28234, TMS320F28234-Q1, TMS320F28232, TMS320F28232-Q1
SPRS439Q – JUNE 2007 – REVISED AUGUST 2022

TMS320F2833x, TMS320F2823x Real-Time Microcontrollers

1 Features

- High-performance static CMOS technology
  - Up to 150 MHz (6.67-ns cycle time)
  - 1.9-V/1.8-V core, 3.3-V I/O design
- High-performance 32-bit CPU (TMS320C28x)
  - IEEE 754 single-precision Floating-Point Unit (FPU) (F2833x only)
  - 16 × 16 and 32 × 32 MAC operations
  - 16 × 16 dual MAC
  - Harvard bus architecture
  - Fast interrupt response and processing
  - Unified memory programming model
  - Code-efficient (in C/C++ and Assembly)
- Six-channel DMA controller (for ADC, McBSP, ePWM, XINTF, and SARAM)
- 16-bit or 32-bit External Interface (XINTF)
  - More than 2M × 16 address reach
- On-chip memory
  - F28335, F28333, F28235: 256K × 16 flash, 34K × 16 SARAM
  - F28334, F28234: 128K × 16 flash, 34K × 16 SARAM
  - F28332, F28232: 64K × 16 flash, 26K × 16 SARAM
  - 1K × 16 OTP ROM
- Boot ROM (8K × 16)
  - With software boot modes (through SCI, SPI, CAN, I2C, McBSP, XINTF, and parallel I/O)
  - Standard math tables
- Clock and system control
  - On-chip oscillator
  - Watchdog timer module
- GPIO0 to GPIO63 pins can be connected to one of the eight external core interrupts
- Peripheral Interrupt Expansion (PIE) block that supports all 58 peripheral interrupts
- 128-bit security key/lock
  - Protects flash/OTP/RAM blocks
  - Prevents firmware reverse-engineering
- Enhanced control peripherals
  - Up to 18 PWM outputs
  - Up to 6 HRPWM outputs with 150-ps MEP resolution
  - Up to 6 event capture inputs
  - Up to 2 Quadrature Encoder interfaces
  - Up to 8 32-bit timers (6 for eCAPs and 2 for eQEPs)
  - Up to 9 16-bit timers (6 for ePWMs and 3 XINTCTRs)
- Three 32-bit CPU timers
- Serial port peripherals
  - Up to 2 CAN modules
  - Up to 3 SCI (UART) modules
  - Up to 2 McBSP modules (configurable as SPI)
  - One SPI module
  - One Inter-Integrated Circuit (I2C) bus
- 12-bit ADC, 16 channels
  - 80-ns conversion rate
  - 2 × 8 channel input multiplexer
  - Two sample-and-hold
  - Single/simultaneous conversions
  - Internal or external reference
- Up to 88 individually programmable, multiplexed GPIO pins with input filtering
- JTAG boundary scan support
  - IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture
- Advanced debug features
  - Analysis and breakpoint functions
  - Real-time debug using hardware
- Development support includes
  - ANSI C/C++ compiler/assembler/linker
  - Code Composer Studio™ IDE
  - DSP/BIOS™ and SYS/BIOS
  - Digital motor control and digital power software libraries
- Low-power modes and power savings
  - IDLE, STANDBY, HALT modes supported
  - Disable individual peripheral clocks
- Endianness: Little endian
- Package options:
  - Lead-free, green packaging
  - 176-ball plastic Ball Grid Array (BGA) [ZJZ]
  - 179-ball MicroStar BGA™ [ZHH]
  - 179-ball New Fine Pitch Ball Grid Array (nFBGA) [ZAY]
  - 176-pin Low-Profile Quad Flatpack (LQFP) [PGF]
  - 176-pin Thermally Enhanced Low-Profile Quad Flatpack (HLQFP) [PTP]
- Temperature options:
  - A: –40°C to 85°C (PGF, ZHH, ZAY, ZJZ)
  - S: –40°C to 125°C (PTP, ZJZ)
  - Q: –40°C to 125°C (PTP, ZJZ) (AEC Q100 qualification for automotive applications)

3.1 Functional Block Diagram

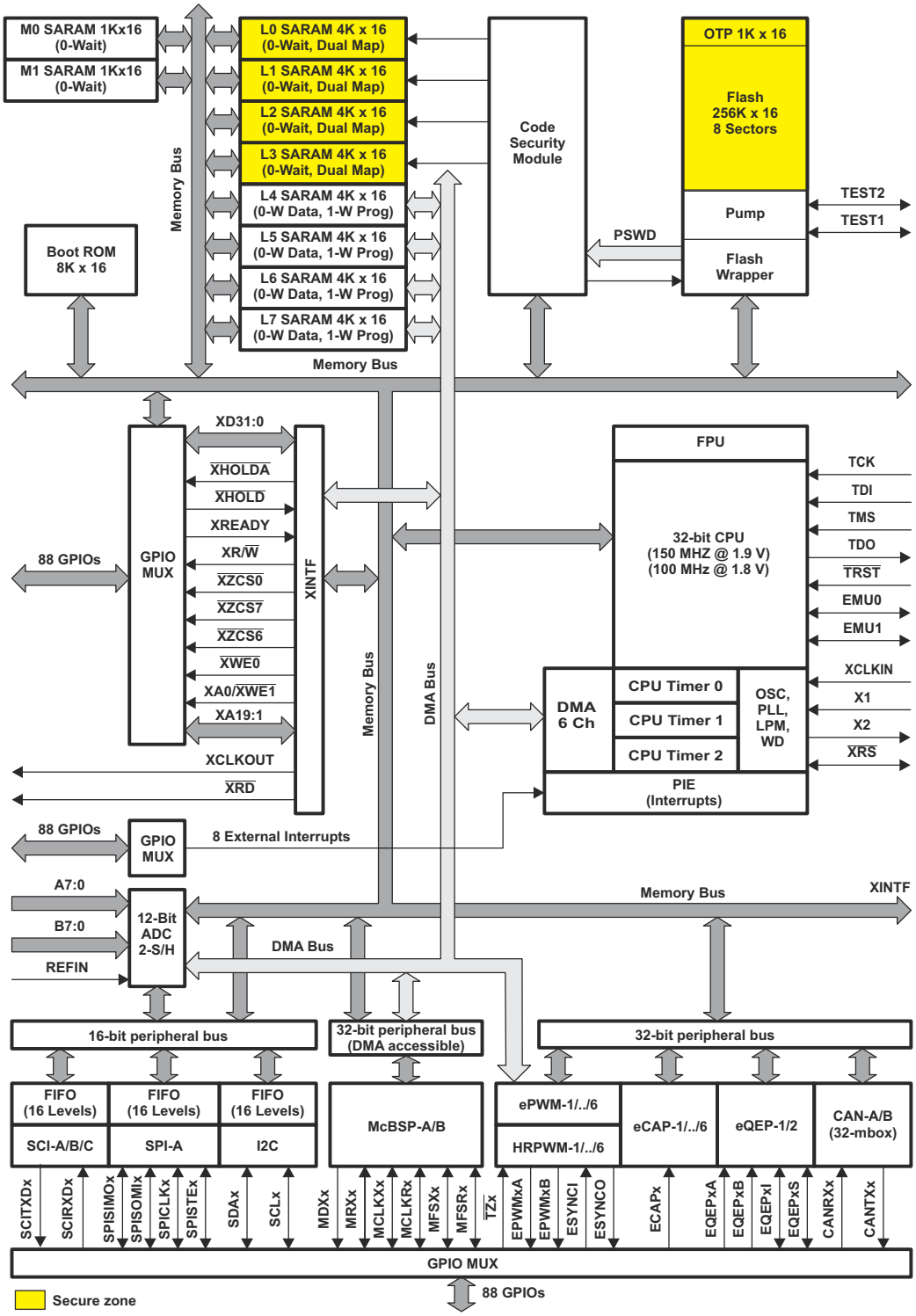

Figure 3-1. Functional Block Diagram